Series Editor
Bernard Multon

Power Electronics Applied to Industrial Systems and Transports

Volume 2
Power Converters and their Control

Nicolas Patin

iSTE PRESS
ELSEVIER

First published 2015 in Great Britain and the United States by ISTE Press Ltd and Elsevier Ltd

ISTE Press Ltd
27-37 St George's Road
London SW19 4EU
UK

www.iste.co.uk

Elsevier Ltd
The Boulevard, Langford Lane
Kidlington, Oxford, OX5 1GB
UK

www.elsevier.com

Notices

Knowledge and best practice in this field are constantly changing. As new research and experience broaden our understanding, changes in research methods, professional practices, or medical treatment may become necessary.

Practitioners and researchers must always rely on their own experience and knowledge in evaluating and using any information, methods, compounds, or experiments described herein. In using such information or methods they should be mindful of their own safety and the safety of others, including parties for whom they have a professional responsibility.

To the fullest extent of the law, neither the Publisher nor the authors, contributors, or editors, assume any liability for any injury and/or damage to persons or property as a matter of products liability, negligence or otherwise, or from any use or operation of any methods, products, instructions, or ideas contained in the material herein.

British Library Cataloguing in Publication Data
A CIP record for this book is available from the British Library
Library of Congress Cataloging in Publication Data
A catalog record for this book is available from the Library of Congress
ISBN 978-1-78548-001-0

Printed and bound in the UK and US

Preface

Volume 2 of this series gives an overview of electronic power converters (DC/DC, DC/AC, AC/DC and AC/AC) as used in industrial and transport applications, notably in variable speed drives. Existing works used in teaching on the subject have paid little attention to the detailed analysis of vector pulse width modulation (PWM) for three-phase inverters, including their impact on the DC power bus. We will attempt to provide this analysis, alongside a presentation of matrix converters (AC/AC conversion) and an introduction to multi-level converters. This volume will also include a case study of the design of a variable speed drive, which constitutes a synthesis of the other subjects tackled in the book (with the exception of direct AC/AC conversion).

This volume also contains two appendices, providing a general formula for electrical engineering and power electronics, and a relatively thorough discussion of the spectrum analysis tools used in power electronics. The formulas supplied in Appendix 1 use elements of electromagnetism which are not covered in this volume; this appendix is, in fact, intended for use with all four volumes of the book. Volume 4 [PAT 15c] is particularly concerned with electromagnetic compatibility, providing a presentation of

radiation disturbances, which requires the use of certain electromagnetic notions. Generally speaking, all chapter references in the appendices specify the volume in question.

Nicolas PATIN
Compiègne, France
February 2015

1

DC/DC Converters

1.1. DC motors

1.1.1. *Electromechanical model*

A direct current (DC) machine consists of two distinct elements:

– an armature containing a coil, located at the rotor;

– a field coil (or magnets fulfilling the same function) at the stator.

The presence of the field coil means that the armature coil operates within a magnetic flux of ψ_f. When a current i_a is supplied to the armature, is enabled electromechanical energy conversion by creating a motor torque of the form:

$$t_m = k.\psi_f.i_a \qquad [1.1]$$

where k is a constant which is characteristic of the machine. Furthermore, we note that the flux ψ_f is:

– either a function of the current i_{exc} circulating in the field coil, if this exists (more precisely, a linear function for a non-saturated machine: $\psi_f = K_\phi.i_{exc}$);

– or a constant $\psi_f = \Psi_f$ in the case of an inductor using permanent magnets.

Due to energy conversion, it is possible to establish that the mechanical and electrical instantaneous powers are identical. Consequently, the machine holds an electromotive force (e.m.f.) e_a such that:

$$e_a.i_a = t_m.\omega \qquad [1.2]$$

where ω is the rotation speed of the machine expressed in rad/s. Thus, we obtain:

$$e_a = k.\psi_f.\omega \qquad [1.3]$$

As the armature contains a wound coil, we inevitably encounter a resistance R_a and an inductance L_a: consequently, the equivalent electrical model of the DC motor is a series circuit (R_a, L_a, e_a). For the purposes of our study in the remainder of this chapter, we will use the hypothesis of negligible resistance; consequently, the model of the machine is reduced to a series circuit (L_a, e_a), and the mechanical inertia J_m of the motor is such that, on the scale of the switching period T_d of the converter (i.e. operating period of the switch), the speed ω may be considered constant (slow evolution across a high number of switching periods – typically, the mechanical time constant of the machine will be around 100 times larger than T_d). Finally, all of our converter studies will be carried out in a steady state, i.e. all of the electrical values (currents and voltages) will be periodical. This hypothesis allows us to postulate that as the voltage V_L at the terminals of inductance L is written as a function of current I_L as follows:

$$V_L(t) = L\frac{dI_L}{dt} \qquad [1.4]$$

then we must have

$$\langle V_L \rangle_{T_d} = \frac{1}{T_d}\int_{(T_d)} V_L(t)\,dt = 0. \qquad [1.5]$$

1.1.2. *Applications*

Mechanical applications are characterized in terms of mechanical couple and speed reversibility; operations are qualified by the number of quadrants used in the torque/speed reference frame. As we see from equations [1.1] and [1.3], there is a direct correspondence between the torque/speed and current/voltage reference frames.

The cases encountered in practice correspond to five different types of converters (choppers):

– one-quadrant chopper, with a single rotation direction in a motor function (step-down chopper);

– one-quadrant chopper, with a single rotation direction in a generating function (step-up chopper);

– two-quadrant chopper, with a single rotation direction for motor or generator functions (current-reversible two-quadrant chopper);

– two-quadrant chopper, with two rotation directions but only one torque – motor or generator direction (voltage-reversible two-quadrant chopper);

– four-quadrant chopper, with two rotation directions and two torques – motor or generator directions (four quadrant, i.e. full bridge chopper).

1.2. Step-down chopper

1.2.1. *Structure and general equation model*

The structure of a step-down chopper is shown in Figure 1.4. This is a single quadrant converter, used to operate a DC motor in rotor mode with a single rotation direction.

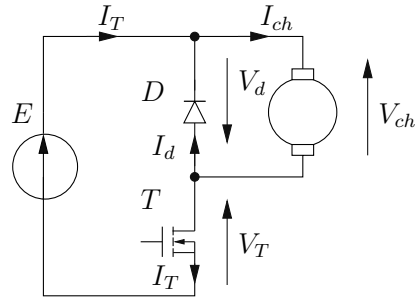


Figure 1.1. *Single quadrant chopper (step-down chopper)*

The equation model of the circuit is based on two independent loops and one node:

$$\begin{cases} E = V_T - V_d \\ -V_d = V_{load} \\ I_{load} = I_T + I_d \end{cases} \quad [1.6]$$

1.2.2. *Continuous conduction*

In the case of continuous conduction, the operation of the converter over a switching period T_d is split into two distinct phases, with durations of $\alpha.T_d$ (T ON, D OFF) and $(1-\alpha).T_d$ (T OFF, D ON), respectively.

During the first phase, we control transistor switch-off. Consequently,

$$V_T = 0 \quad [1.7]$$

hence:

$$V_d = -E \quad [1.8]$$

As the voltage at the diode terminals is negative, the diode is switched off:

$$I_d = 0 \quad [1.9]$$

hence:

$$I_T = I_{load} \quad [1.10]$$

This also gives us:

$$V_{load} = E \quad [1.11]$$

In the case of an (L_a, e_a) modeling of the DC motor, supposing that $e_a = E_a = cte$, we may note:

$$L_a \frac{dI_{load}}{dt} = E - E_a \quad [1.12]$$

hence:

$$I_{load}(t) = I_{load}(0) + \frac{E - E_a}{L_a}(t) \quad [1.13]$$

At the end of this phase, we may write:

$$I_{load}(\alpha.T_d) = I_{load}(0) + \frac{E - E_a}{L_a}(\alpha.T_d) \quad [1.14]$$

and the value of $I_{load}(0)$ is, in accordance with the definition of continuous conduction, non-null.

During the second phase, we control transistor switch-on. Hence:

$$I_T = 0 \quad [1.15]$$

At the start of this phase, as I_{load} is non-null and cannot be subject to discontinuity, the diode is switched on:

$$I_d = I_{load} \quad [1.16]$$

We, therefore, write:

$$V_d = 0 \quad [1.17]$$

and, in the load:

$$V_{load} = 0 \quad [1.18]$$

and:

$$V_T = E \quad [1.19]$$

The evolution of the current in the load is, therefore, written as:

$$I_{load}(t) = I_{load}(\alpha.T_d) - \frac{E_a}{L_a}(t - \alpha.T_d) \quad [1.20]$$

Given that the circuit is operating in permanent mode, we note that the voltage at the terminals of the inductance L_a of the machine $V_{load} - E_a$ presents an average value of zero for the switching period T_d; hence:

$$\begin{aligned}\langle V_{load} - E_a \rangle_{T_d} &= \frac{1}{T_d}\left(\int_0^{\alpha.T_d}(E - E_a)dt + \int_{\alpha.T_d}^{T_d}(-E_a)\,dt\right) \\ &= \frac{1}{T_d}\left(\alpha.T_d.(E - E_a) - (1-\alpha)\,.T_d.\,(E_a)\right)) = 0 \quad [1.21]\end{aligned}$$

hence:

$$E_a = \alpha.E \quad [1.22]$$

Once this equation is established, we may rewrite the evolution of current I_{load} over the two phases of the switching period. For the first phase, the current increases:

$$I_{load}(t) = I_{load}(0) + \frac{(1-\alpha).E}{L_a}t \qquad [1.23]$$

For the second phase, the current decreases, as follows:

$$I_{load}(t) = I_{load}(\alpha.T_d) - \frac{\alpha.E}{L_a}(t - \alpha.T_d) \qquad [1.24]$$

Given the periodicity of the current and its piecewise affine evolution, current $I_{load}(0)$ is the minimum value I_{min} of the current, whilst $I_{load}(\alpha.T_d)$ is its maximum value I_{max}. Based on results [1.56] and [1.57], it is possible to establish an expression of the ripple of the current $\Delta I_{load} = I_{max} - I_{min}$ as a function of E, L_a and T_d (where $F_d = \frac{1}{T_d}$):

$$\Delta I_{load} = \frac{\alpha.(1-\alpha)T_d.E}{L_a} = \frac{\alpha.(1-\alpha).E}{L_a.F_d} \qquad [1.25]$$

The waveforms corresponding to the results established above are shown in Figure 1.2.

A link between electrical and mechanical quantities can now be established if the load is perfectly known. We have seen that the e.m.f. E_a imposed on the DC motor by the chopper is expressed as $\alpha.E$. Consequently, the chopper imposes the speed ω of the machine, in accordance with equation [1.3]. This speed corresponds to a resistive torque c_r of the load (dry, viscous or aeirodynamic friction, load to raise using a lift, etc.). As the machine is operating in permanent mode (with a speed which is presumed to be constant, or at least varying slowly), we know, based on the fundamental

principle of dynamics, that the motor torque is equal to the resistive torque:

$$c_m - c_r = J_T \frac{d\omega}{dt} = 0 \Rightarrow c_m = c_r \qquad [1.26]$$

where J_t is the inertia of the machine and its load. Given the resistive torque $c_r = C_r = cte$ (and thus c_m), using equation [1.1], we may calculate the induced current i_a of the machine, which, in this case, is simply the average value of $I_{load}(t)$, which we will denote as I_0.

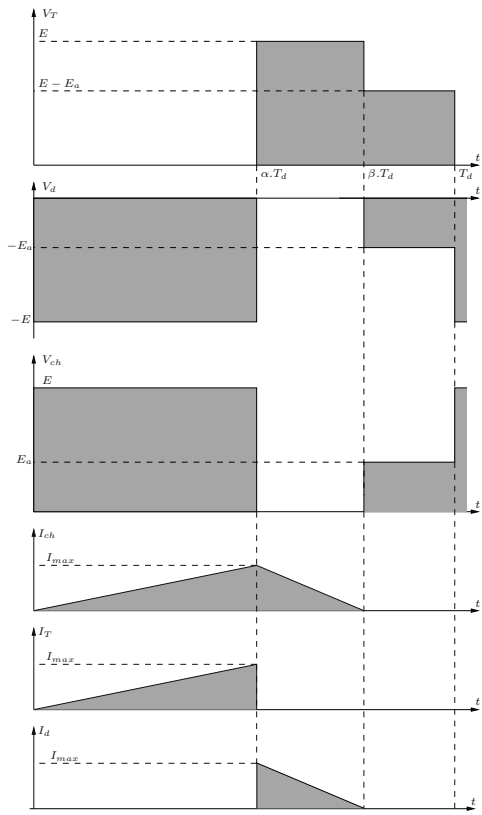


Figure 1.2. *Waveforms for a step-down chopper with alternating current*

The key values involved in continuous conduction operation of this chopper are shown in Table 1.1.

Element	*Value or temporal expression*
Max. transistor voltage V_{Tmax}	E
Max. reverse diode voltage V_{dmax}	$-E$
Average load current I_0	$\frac{C_r}{k.\psi_f}$
Current ripple in the load ΔI_{load}	$\frac{\alpha.(1-\alpha).E}{L_a.F_d}$
Average voltage at load terminals $\langle V_{load} \rangle$	$(\alpha)\,.E$
Max. current in the transistor and diode	$I_0 + \frac{\Delta I_{load}}{2}$
Average current in the transistor $\langle I_T \rangle$	$\alpha.I_0$
Average current in the diode $\langle I_d \rangle$	$(1-\alpha)\,.I_0$
RMS current in the transistor (for $\Delta I_{load} \ll I_0$)	$\sqrt{\alpha}.I_0$
RMS current in the diode (for $\Delta I_{load} \ll I_0$)	$\sqrt{1-\alpha}.I_0$

Table 1.1. *Summary of continuous conduction in a step-down chopper*

1.2.3. *Discontinuous conduction*

In the case of discontinuous conduction, our study is complicated by the fact that the end of the second phase (conducting diode) does not coincide with the end of the switch period. The average current in the load is too low, so the current decreases to zero; this leads to spontaneous turn-off of the diode, while the transistor is not yet at turn-on point. Within time interval $[0, T_d]$, we can, therefore, define an instant $\alpha.T_d$ corresponding to the end of conduction in the transistor, and an instant $\beta.T_d$ (with $\beta \leq 1$) when the diode turns off spontaneously (in the case where $\beta = 1$, we speak of *critical conduction*, which constitutes the limit separating direct and alternating current (AC)). The values and expressions of the different elements used in the first two

phases are identical to those established for DC (noting that $I_{load}(0) = I_{min} = 0$ in this case). During the third phase, both the transistor and the diode are turned off. This gives us:

$$I_T = I_d = 0 \qquad [1.27]$$

As current I_{load} is also identically null, its derivative in relation to time is identically null. We can, therefore, write:

$$I_T = I_d = 0 \qquad [1.28]$$

As current I_{load} is also identically null, its derivative in relation to time is identically null. We can, therefore, write:

$$V_{load} = E_a \qquad [1.29]$$

and thus,

$$\begin{cases} V_d = -E_a \\ V_T = E - E_a \end{cases} \qquad [1.30]$$

The new waveforms for this mode of operation are shown in Figure 1.2.

One way of analyzing this operating mode would be to calculate coefficient β; however, it is generally better to use reasoning based on average input P_e and output power P_s at the switching period scale. As the converter does not contain a storage element, the input power is equal to the output power[1]. Our aim in this case is to calculate the expression of the average voltage $\langle V_{load} \rangle = E_a$ applied to the machine; contrary to the case of DC, this expression will no longer simply be a function of E and α, but also of the average current I_0 in the machine.

1 Even if a storage element were used, the power balance would be null based on the hypothesis of a steady state.

To do this, we note:

$$P_s = \langle V_{load} \rangle .I_0 = E_a.I_0 \qquad [1.31]$$

and

$$\begin{aligned} P_e = E.\langle I_T \rangle &= E \cdot \frac{1}{T_d} \int_0^{\alpha.T_d} \frac{E - E_a}{L_a} t.dt \\ &= E \cdot \frac{\alpha^2.(E - E_a)}{2L_a.F_d} \end{aligned} \qquad [1.32]$$

hence:

$$E_a = \frac{E}{1 + \frac{2L_a.F_d.I_0}{\alpha^2.E}} \qquad [1.33]$$

This result clearly shows that the output voltage depends on α, E and I_0. To analyze this characteristic, we may use the following reduced variables:

$$\begin{cases} x = \frac{2L_a.F_d.I_0}{E} \\ y = E_a/E \end{cases} \qquad [1.34]$$

This leads us to rewrite equation [1.33] as follows:

$$y = \frac{1}{1 + \frac{x}{\alpha^2}} \qquad [1.35]$$

Comparing the latter with the equivalent characteristic in continuous mode, which is simply written as:

$$y = \alpha \qquad [1.36]$$

We may then trace a network of characteristics of y as a parameterized function of x following α; first, however, we must identify the respective domains of validity of equations [1.37] and [1.36]. To do this, we need to determine a critical

function zone. The critical zone simultaneously verifies the two characteristics, as it constitutes the border between the two operating modes. In order to identify this zone, we must simply eliminate parameter α from equation [1.37], replacing it with y in accordance with equation [1.36]. This gives us:

$$y = \frac{1}{1 + \frac{x}{y^2}} = \frac{y^2}{y^2 + x} \qquad [1.37]$$

or:

$$y^2 - y + x = 0 \qquad [1.38]$$

We can easily verify that this zone passes through coordinates $(0, 0)$ and $(1, 0)$ in the plane (x, y) and takes the form of a parabola, with symmetry along the axis with equation $y = 1/2$. We can also show that, on this axis, it passes through point $(1/4, 1/2)$, as shown in Figure 1.3.

1.3. Step-up choppers

1.3.1. *Structure and general equation model*

The structure of a step-up chopper is shown in Figure 1.4. Like the step-down chopper, the step-up chopper is a single quadrant converter, but it operates in the opposite direction: the continuous current motor acts as a generator with this type of converter (still with a single direction of rotation).

Once again, the equation model of this circuit is based on two loops and one junction:

$$\begin{cases} E = V_T - V_d \\ V_T = V_{load} \\ I_{load} = I_T + I_d \end{cases} \qquad [1.39]$$

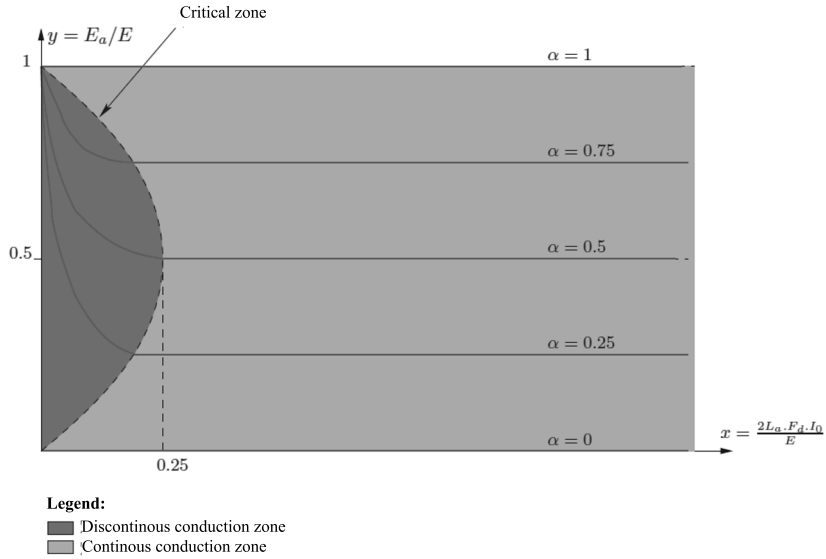


Figure 1.3. *Full reduced characteristic of the step-down chopper (continuous and discontinuous conduction)*

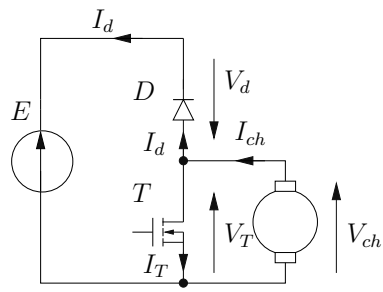


Figure 1.4. *Single quadrant chopper (step-up chopper)*

1.3.2. *Continuous conduction study*

Using the same approach as for the step-down chopper, the switching period T_d begins with a transistor conduction phase of duration $\alpha.T_d$:

$$V_T = 0 \qquad [1.40]$$

hence:

$$V_d = -E \quad [1.41]$$

As the voltage at the diode terminals is negative, the diode is turned off:

$$I_d = 0 \quad [1.42]$$

hence

$$I_T = I_{load} \quad [1.43]$$

and

$$V_{load} = 0 \quad [1.44]$$

In the case of an (L_a, e_a) model of the DC motor (Note, according to the active sign convention, the machine behaves as a generator) for which we presume that $e_a = E_a = cte$, we may note:

$$L_a \frac{dI_{load}}{dt} = E_a \quad [1.45]$$

hence:

$$I_{load}(t) = I_{load}(0) + \frac{E}{L_a} t \quad [1.46]$$

At the end of this phase, we may write:

$$I_{load}(\alpha.T_d) = I_{load}(0) + \frac{E}{L_a} \alpha.T_d \quad [1.47]$$

and once again, we take $I_{load}(0) \neq 0$ due to the definition of continuous conduction.

In the second phase, we control the turn-off of the transistor. Thus,

$$I_T = 0 \quad [1.48]$$

hence, at the beginning of this phase, as I_{load} is non-null and cannot be subject to discontinuity, the diode is turned on:

$$I_d = I_{load} \quad [1.49]$$

Thus, we write:

$$V_d = 0 \quad [1.50]$$

and at the load terminals

$$V_{load} = E \quad [1.51]$$

and

$$V_T = E \quad [1.52]$$

Thus, the evolution of the current in the load is written as:

$$I_{load}(t) = I_{load}(\alpha.T_d) + \frac{E_a - E}{L_a}(t - \alpha.T_d) \quad [1.53]$$

Given that the current operates in a steady state, we may note that the voltage across the inductance L_a of the machine $E_a - V_{load}$ presents an average value of zero over the switching period T_d and thus:

$$\begin{aligned}\langle V_{load} - E_a \rangle_{T_d} &= \frac{1}{T_d}\left(\int_0^{\alpha.T_d} E_a dt + \int_{\alpha.T_d}^{T_d} (E_a - E)\, dt\right) \\ &= \frac{1}{T_d}\left(\alpha.T_d.E_a - (1-\alpha).T_d.(E_a - E)\right) = 0 \quad [1.54]\end{aligned}$$

hence

$$E = \frac{E_a}{1-\alpha} \qquad [1.55]$$

If we consider that the machine is placed at the input point of the converter, and the voltage source E at the output point, note that this corresponds to the direction of power transfer, and in this case, the chopper acts as a boost converter. If we consider the relationship in the same direction as for the step-down chopper, we obtain:

$$E_a = (1-\alpha).E \qquad [1.56]$$

While relationship [1.55] is logical from a physical point of view in terms of system orientation, it is not relevant in the context of the chopper in question, as voltage E is imposed by a source (unless it is designed to absorb energy with no effect on its value). This relationship will be more useful when considering boost switch-mode power supplies, based on this chopper structure, which will be presented in Volume 3 [PAT 15b].

Once this relationship has been established, we can rewrite the evolution of the current I_{load} during the two phases of the switching period. For the first phase, the expression is unchanged, and corresponds to an increase in the current:

$$I_{load}(t) = I_{load}(0) + \frac{(1-\alpha).E}{L_a}t \qquad [1.57]$$

For the second phase, the current decreases as follows:

$$I_{load}(t) = I_{load}(\alpha.T_d) - \frac{\alpha.E}{(1-\alpha).L_a}(t-\alpha.T_d) \qquad [1.58]$$

The waveforms corresponding to these results are shown in Figure 1.5.

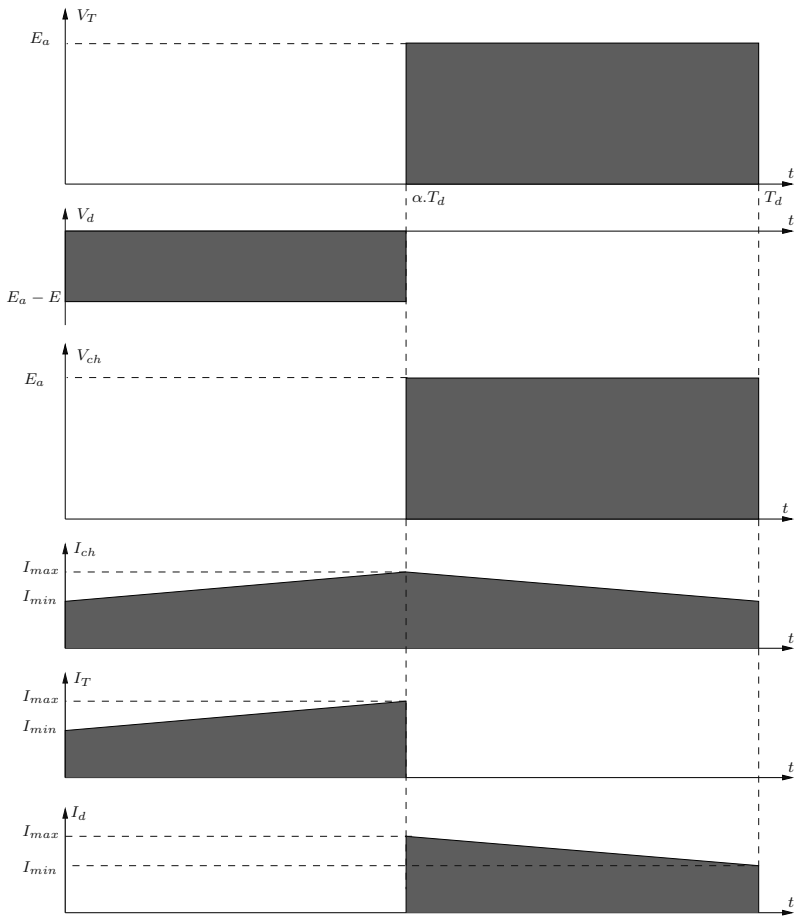


Figure 1.5. *Waveforms for a step-up chopper in continuous conduction*

The key elements in the operation of this chopper in continuous conduction are shown in Table 1.2.

1.3.3. *Discontinuous conduction*

We can carry out the same reasoning for discontinuous conduction as for the step-down chopper, using an equality between power P_e on the machine side and P_s on the side of

source E. Current I_{load} always increases during the transistor conduction phase, but this time with an initial value of zero:

$$I_{load}(t) = \frac{E_a}{L_a} t \qquad [1.59]$$

to reach a maximum value of $I_{max} = \frac{\alpha E_a T_d}{L_a}$ in the final instant of this phase ($t = \alpha.T_d$).

Element	*Value or temporal expression*
Max. transistor voltage V_{Tmax}	E
Max. reverse diode voltage V_{dmax}	$-E$
Average load current I_0	$\frac{C_{brake} - C_r}{k.\psi_f}$
Current frequency in the load ΔI_{load}	$\frac{\alpha.E_a}{L_a.F_d} = \frac{\alpha.(1-\alpha).E}{L_a.F_d}$
Average voltage at load terminals $\langle V_{load} \rangle = E_a$	$(1-\alpha).E$
Max. current in the transistor and diode	$I_0 + \frac{\Delta I_{load}}{2}$
Average current in the transistor $\langle I_T \rangle$	$\alpha.I_0$
Average current in the diode $\langle I_d \rangle$	$(1-\alpha).I_0$
RMS current in the transistor (for $\Delta I_{load} \ll I_0$)	$\sqrt{\alpha}.I_0$
RMS current in the diode (for $\Delta I_{load} \ll I_0$)	$\sqrt{1-\alpha}.I_0$

Table 1.2. *Summary of continuous conduction in a step-up chopper*

The current decreases during the diode conduction phase, and we wish to determine the instant $\beta.T_d$ when I_{load} cancels out. To do this, we use $\delta.T_d = (\beta - \alpha).T_d$ and thus:

$$I_{max} + \frac{E_a - E}{L_a} \delta.T_d = 0 \qquad [1.60]$$

hence:

$$\delta = \frac{\alpha.E_a}{E - E_a} \qquad [1.61]$$

For reference, during the third phase of the switching period (diode and transistor turned off), we have:

$$\begin{cases} V_T = E_a \\ V_d = E_a - E \\ V_{load} = E_a \end{cases} \quad [1.62]$$

The waveforms associated with this operating mode are presented in Figure 1.6.

As in the case of continuous conduction, ***E*** is fixed for the target application (i.e. a chopper supplying a DC motor). Consequently, the expression of the ratio $y = E_a/E$ is preferable to E/E_a, as in the case of boost power supplies, which will be presented later. Thus, we may rewrite δ as follows:

$$\delta = \frac{\alpha.y}{1-y} \quad [1.63]$$

If we wish to determine the operating point of the chopper, this must be characterized in relation to the average current in the machine, i.e.:

$$\begin{aligned} \langle I_{load} \rangle = I_0 &= \frac{(\alpha+\delta).I_{max}}{2} = \frac{\alpha}{1-y} \cdot \frac{I_{max}}{2} \\ &= \frac{\alpha^2 E_a}{2.L_a F_d (1-y)} \end{aligned} \quad [1.64]$$

Using the same reduced current $x = \frac{2L_a F_d I_0}{E}$ as for the step-down chopper, we obtain:

$$x = \frac{\alpha^2 y}{1-y} \quad [1.65]$$

and seeking the expression of $y(x)$, we obtain:

$$y = \frac{x}{\alpha^2 + x} \qquad [1.66]$$

Equation [1.56] may be rewritten with reduced variable y as follows:

$$y = 1 - \alpha \qquad [1.67]$$

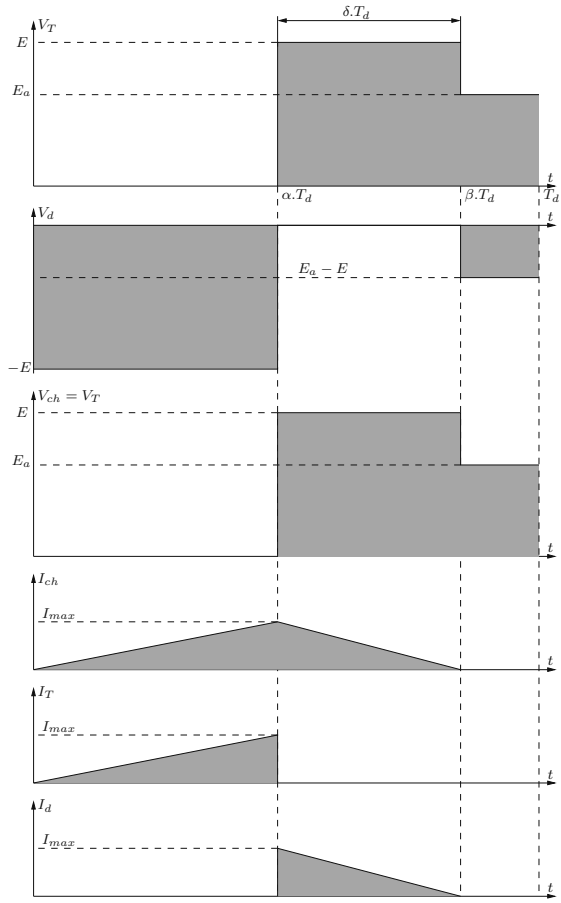


Figure 1.6. *Waveforms for a step-up chopper in discontinuous conduction*

Following the same approach used for the step-down chopper, we identify the critical zone separating the continuous and discontinuous operating modes, replacing α with its expression $1 - y$ in accordance with [1.66] in [1.67]:

$$y = \frac{x}{(1-y)^2 + x} \qquad [1.68]$$

This gives us the following equation for the critical zone:

$$x = y.(1-y) \qquad [1.69]$$

This is identical to the critical zone equation for the step-down chopper. In fact, the network of reduced characteristics for the step-up chopper is exactly symmetrical to that of the step-down chopper in the plane with equation $y = 1/2$, as we see in Figure 1.7.

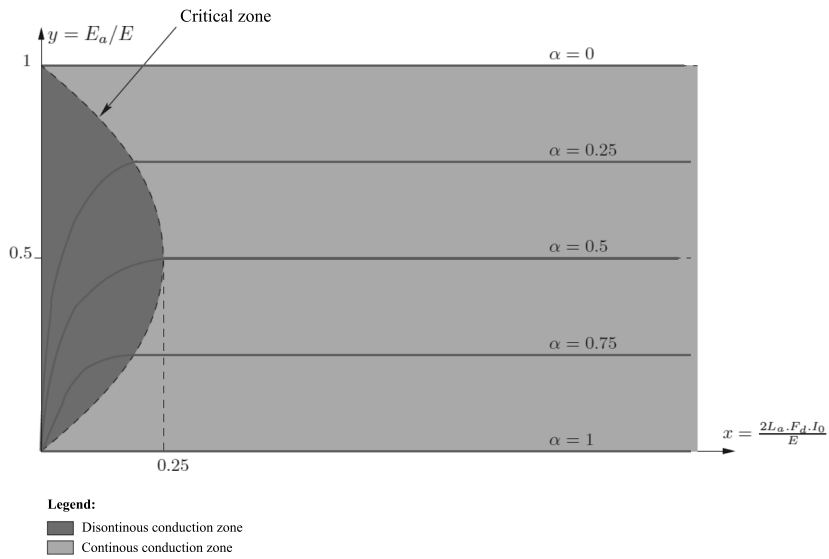


Figure 1.7. *Full reduced characteristic of a step-up chopper (continuous and discontinuous conduction)*

1.4. Two-quadrant current-reversible chopper

1.4.1. *Structure and general equation model*

The converter structure shown in Figure 1.8 is a current-reversible two-quadrant chopper, which is effectively a combination of the step-down and step-up choppers seen above. In this section, therefore, we will not present continuous and discontinuous operating modes, as these correspond to our calculations in sections 1.2 and 1.3. Instead, we will focus on the way in which a converter control allows transparent passage from the step-down to the step-up chopper during a normal operating phase of a continuous current machine (e.g. braking).

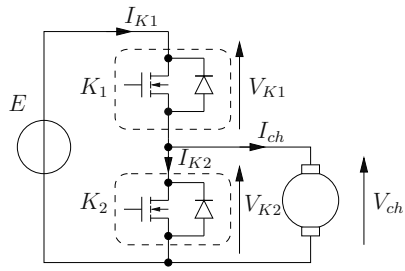


Figure 1.8. *Two-quadrant chopper (current reversible)*

As a starting point, when creating an equation model, we may leave aside the precise details of currents in switches K_1 and K_2 (currents in transistors and diodes) to concentrate on currents I_{K1} and I_{K2}, noting that the three-segment switches used allow us to reverse the direction of current. As before (for step-down and step-up choppers), we may write:

$$\begin{cases} E = V_{K1} + V_{K2} \\ V_{K2} = V_{load} \\ I_{load} = I_{K1} - I_{K2} \end{cases} \qquad [1.70]$$

1.4.2. *Step-up and step-down operation*

Using classic chopper control methods, we send complementary orders to the gates of both transistors. One key rule which must be respected is that both transistors should never be closed simultaneously. As an additional precaution, the transistor switching times are not always identical, and are precisely controlled: a deadtime T_M is established between the order to open one transistor and the order to close the other. This guarantees the absence of simultaneous conduction. The circulation of current I_{load} in the load is maintained by one of the two diodes in the circuit:

– the upper diode (in K_1) is on if $I_{load} < 0$ (step-up chopper operation);

– the lower diode (in K_2) is on if $I_{load} > 0$ (step-down chopper operation).

The permanent control of both transistors might be considered superfluous, as, when current I_{load} is positive, only the transistor in K_2 may be used, and when I_{load} is negative, only K_1 may be used. However, the control of both components is generally preferred, for two reasons:

– the passage through the point of zero current is managed transparently: as the transistors are under permanent control, the transistor which is not operating before the passage through zero is switched on without needing to establish a control principle detecting current reversal[2]. This also avoids control delays;

– a metal oxide semiconductor field effect transistor (MOSFET) is bidirectional in terms of current, and is generally a better conductor than the parallel diode. This provides considerable gains in terms of efficiency, particularly

2 This is generally known as *switching logic*, and is also used in controlling thyristor rectifiers.

at very low voltages (in which case, we may speak of a synchronous rectifier). The anti-parallel diode, therefore, only acts as a transitional free wheel during deadtime periods.

Using the hypothesis of transistors which are genuinely unidirectional in terms of current (such as insulated gate bipolar transistors (IGBTs)), Figure 1.9 presents the waveforms of current through the load and the conduction intervals of different components.

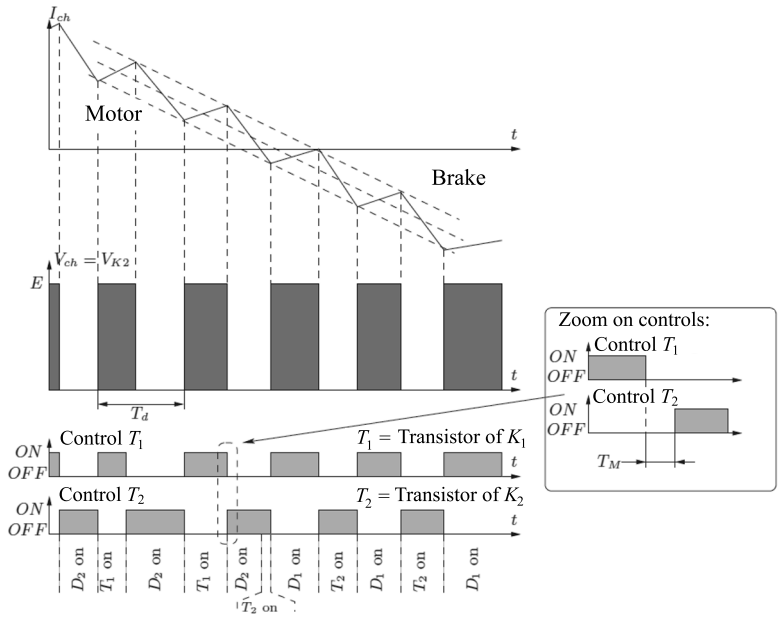


Figure 1.9. *Waveforms and switch conduction sequence for the two-quadrant (current reversible) chopper*

NOTE 1.1.– The structure (K_1, K_2) made up of the two transistors and two diodes is known as a *half-bridge*. This structure is widely used in a range of components (choppers, inverters, controlled rectifiers, etc.), and is commercially available in the form of integrated power modules. This assembly may be considered as the *basic structure in power electronics*.

1.5. Two-quadrant voltage-reversible chopper

1.5.1. *Structure and general equation model*

The converter shown in Figure 1.10 is a two-quadrant voltage-reversible chopper, with a single authorized direction of current on the load (machine) side. The equation model of this converter is partially based on the expression of voltage V_{load} as a function of voltages V_{d1} and V_{T2}:

$$V_{load} = -V_{d1} - V_{T2} \qquad [1.71]$$

and we note that:

$$\begin{cases} E = V_{T1} - V_{d1} \\ E = -V_{d2} + V_{T2} \end{cases} \qquad [1.72]$$

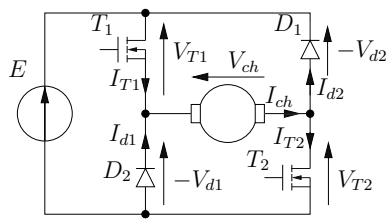


Figure 1.10. *Two-quadrant chopper (voltage reversible)*

The model is also based on equations related to currents:

$$\begin{cases} I_{load} = I_{T1} + I_{D1} \\ I_{load} = I_{T2} + I_{D2} \\ I_e = I_{T1} - I_{D2} \end{cases} \qquad [1.73]$$

where I_e is the output current of the voltage source E.

1.5.2. *Operating principle*

As we have two controlled switches (both with two possible states ON and OFF), we have four possible configurations for the full converter. We will limit our study to the continuous conduction mode (i.e. $I_{load} \neq 0$):

a) T_1 ON and T_2 ON: in this configuration, we may assume that $V_{T1} = V_{T2} = 0$. We, therefore, obtain:

$$\begin{cases} V_{d1} = -E \\ V_{d2} = -E \end{cases} \quad [1.74]$$

and thus the diodes D_1 and D_2 are in the OFF state.

We then note that:

$$V_{load} = E \quad [1.75]$$

Regarding currents, we have:

$$I_{T1} = I_{T2} = I_e = I_{load} \quad [1.76]$$

and

$$I_{d1} = I_{d2} = 0 \quad [1.77]$$

In this configuration, we see that the machine operates as a motor in one sense of rotation, denoted (1), for a positive power supply voltage.

b) T_1 ON and T_2 OFF: in this configuration, we have $V_{T1} = 0$ (T_1 ON) and $I_{T2} = 0$ (T_2 OFF), hence,

$$\begin{cases} V_{d1} = -E \\ I_{d2} = I_{load} \end{cases} \quad [1.78]$$

Diode D_2 is, therefore, in the ON state ($V_{d2} = 0$) for this control input configuration. Hence,

$$V_{load} = 0 \qquad [1.79]$$

The balance of currents in the circuit is as follows:

$$\begin{cases} I_{T1} = I_{d2} = I_{load} \\ I_{T2} = I_{d1} = I_e = 0 \end{cases} \qquad [1.80]$$

This configuration corresponds to a "free wheel" in which the voltage at the terminals of the machine is equal to zero.

c) T_1 OFF and T_2 ON: in this configuration, we have $V_{T2} = 0$ (T_2 ON) and $I_{T1} = 0$ (T_1 OFF), hence,

$$\begin{cases} V_{d2} = -E \\ I_{d1} = I_{load} \end{cases} \qquad [1.81]$$

Diode D_2 is in the ON state ($V_{d2} = 0$) for this control input configuration. Hence,

$$V_{load} = 0 \qquad [1.82]$$

The balance of currents in the circuit is as follows:

$$\begin{cases} I_{T2} = I_{d1} = I_{load} \\ I_{T1} = I_{d2} = I_e = 0 \end{cases} \qquad [1.83]$$

This configuration is also of the "free wheel" type. From a functional perspective, it adds nothing compared to the previous configuration.

d) T_1 OFF and T_2 OFF: in this configuration, we have $I_{T1} = I_{T2} = 0$ (T_1 and T_2 OFF), hence:

$$\begin{cases} I_{d1} = I_{load} \\ I_{d2} = I_{load} \end{cases} \quad [1.84]$$

Diodes D_1 and D_2 are therefore in the ON state ($V_{d1} = V_{d2} = 0$) for this control input configuration. Hence:

$$V_{load} = -E \quad [1.85]$$

The balance of currents in the circuit is as follows:

$$\begin{cases} I_{d1} = I_{d2} = I_{load} \\ I_{T1} = I_{T2} = 0 \\ I_e = -I_{load} \end{cases} \quad [1.86]$$

In this configuration, the machine turns in direction (2), but the current I_{load} continues to circulate in the same direction. The machine, therefore, operates as a generator.

SUMMARY.– This converter allows us to operate a DC motor with a unidirectional torque and two directions of rotation. A typical application of this type of converter is in a crane, where the mechanical load directs operations: the DC motor operates as a motor during lifting, and as a brake during descent. From a control perspective, control inputs (a–b) or (a–c) are applied during lifting (at the scale of a switching period T_d); in descent phases, the controls are of type (d–b) or (d–c).

As we have seen, control configurations b and c are identical from a user perspective, and we may choose to use only one of these configurations. However, from a purely physical perspective, this would lead to overuse of one switch to the detriment of another, meaning that component losses

would become unbalanced. If the more complex implementation involved in alternating both free wheel configurations b and c is acceptable, it is therefore preferable to use this type of control scheme.

1.6. Four-quadrant chopper

1.6.1. *Structure and general equation model*

The converter structure shown in Figure 1.11 is a four-quadrant chopper. This means that the converter allows a DC motor to operate as a motor and as a generator in both directions of rotation. This converter may be seen as an assembly of two two-quadrant choppers: one current-reversible and the other voltage-reversible.

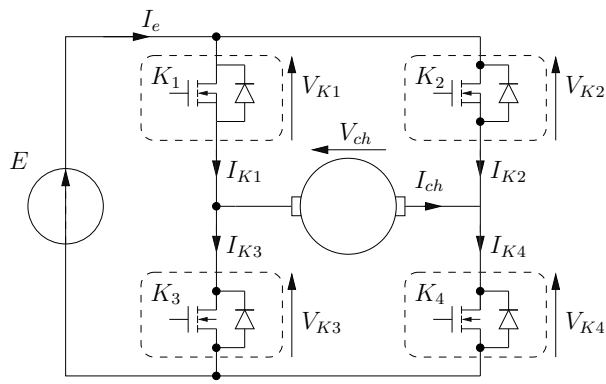


Figure 1.11. *Four-quadrant chopper*

This structure is relatively easy to study, due to the fact that by knowing the switch control input, we are able to know the voltage applied to the load.

If every half-bridge is controlled as defined in section 1.4 for the current-reversible two-quadrant chopper, then the control inputs for K_1 and K_3 on the one hand and K_2 and K_4 on the other hand are complementary (with the introduction

of a deadtime to avoid short-circuiting the source E). Thus, for each half-bridge, we may define a *connection function* c as follows:

$$c = \begin{cases} 0 & \text{if high side transistor is OFF, low side transistor is ON} \\ 1 & \text{if high side transistor is ON, low side transistor is OFF} \end{cases} \quad [1.87]$$

Let c_a be the switching function associated with the half-bridge (K_1, K_3) and c_b the switching function of (K_2, K_4).

Voltage V_{K3} may be expressed as a function of E and c_a alone:

$$V_{K3} = E.c_a \quad [1.88]$$

as, for example, whatever the sign of I_{load}, if $c_a = 0$, the current will circulate in either the transistor ($I_{load} < 0$) or the diode ($I_{load} > 0$) of switch K_3.

In the same way, we note that:

$$V_{K4} = E.c_b \quad [1.89]$$

and thus,

$$V_{load} = E.\,(c_a - c_b) \quad [1.90]$$

The equation model of the currents in this circuit gives us:

$$\begin{cases} I_{K1} = I_{K3} + I_{load} \\ I_{K4} = I_{load} + I_{K2} \\ I_e = I_{K1} + I_{K2} \end{cases} \quad [1.91]$$

We may also express the currents in the switches as a function of I_{load} and the switching functions c_a and c_b:

$$\begin{cases} I_{K1} = I_{load}.c_a \\ I_{K3} = -I_{load}.(1 - c_a) \\ I_{K4} = I_{load}.\,(1 - c_b) \\ I_{K2} = -I_{load}.c_b \end{cases} \quad [1.92]$$

The current I_e supplied by source E is, therefore, expressed as:

$$I_e = I_{K1} + I_{K2} = I_{load}.\,(c_a - c_b) \quad [1.93]$$

1.6.2. *Control strategy*

The results shown in the previous section only apply when using complementary control for transistors in the same half-bridge. On this basis, switching functions c_a and c_b may be chosen independently. However, the chopper can only control one quantity, the voltage V_{load} applied to the machine[3]. If the number of control input values exceeds the number of values to control, a variety of choices are possible. In this case, we speak of control strategies, where each strategy presents a number of advantages and drawbacks which must be taken into consideration when making a selection for a target application.

In this chapter, we will only consider the simplest strategy, which consists of controlling the two half-bridges in a complementary manner. Thus, when $c_a = 0$, we have $c_b = 1$ and vice versa. This strategy is known as *bipolar modulation*. Another widespread strategy is *unipolar modulation*; we will

3 The current I_{load} absorbed by the machine is simply a consequence of this voltage supply (in terms of causality).

consider this strategy in the next chapter in the context of inverters (DC/AC converters), more precisely for the control of a single phase inverter, the power structure of which is identical to that of the four-quadrant chopper.

The complementary control can be summarized as:

$$c_b = 1 - c_a \qquad [1.94]$$

This gives us the following result:

$$V_{load} = E.\,(2c_a - 1) \qquad [1.95]$$

The voltage applied to the load can, therefore, only take the two values $\pm E$, hence the term "bipolar modulation". Concerning the input current into the converter, we have:

$$I_e = I_{load}.\,(2c_a - 1) \qquad [1.96]$$

The current absorbed from source E is, therefore, equal to $\pm I_{load}$.

Returning to the notion of duty cycle α (for a switching period $[0, T_d]$), we have $c_a = 1$ for the interval $[0, \alpha.T_d]$ and $c_a = 0$ for the interval $[\alpha.T_d, T_d]$. We can then evaluate the average voltage at the load terminals $\langle V_{load} \rangle$ and the average current taken from the source $\langle I_e \rangle$:

$$\langle V_{load} \rangle = (2\alpha - 1)\,.E \qquad [1.97]$$

and

$$\langle I_e \rangle = (2\alpha - 1)\,.I_{load} \qquad [1.98]$$

One interesting aspect of this assembly is that operation with discontinuous current is no longer possible. This mode of operation is unsatisfactory, as:

– there is a loss of control (however, short) when the machine is disconnected from the converter (all switches open);

– switches are underused over time. This is due to poor dimensioning (and is genuinely a valid criterion for switch-mode power supplies);

– the behavior of the converter is more complex (the voltage supplied to the machine is not mastered).

However, the magnitude of the waves in voltage V_{load} on the machine side is high ($2.E$), resulting in higher wave magnitude of the current injected into the machine (previously assumed to be constant in calculating $\langle I_e \rangle$). If the evolution of current I_{load} over time interval $[0, \alpha.T_d]$ is written using the hypothesis of an (L_a, E_a) model of the machine, we obtain:

$$I_{load}\,(t) = \frac{E - E_a}{L_a} t + I_{load}\,(t) \qquad [1.99]$$

In the case of a steady state, we know that $I_{load}(0)$ is the minimum current I_{min}, while $I_{load}(\alpha.T_d)$ is the maximum current I_{max}. Consequently, the wave magnitude of current ΔI_{load} is written as:

$$\Delta I_{load} = I_{max} - I_{min} = \frac{E - E_a}{L_a} \alpha.T_d \qquad [1.100]$$

where E_a is equal to the average voltage $\langle V_{load} \rangle$ provided by the converter, the expression of which was established in equation [1.97]. Thus:

$$\Delta I_{load} = \frac{2\alpha\,(1 - \alpha)\,E}{L_a.F_d} \qquad [1.101]$$

We can show that the wave magnitude is highest for $\alpha = 1/2$ (i.e. for $\langle V_{load} \rangle = 0$):

$$\Delta I_{ch\max} = \frac{E}{2L_a.F_d} \qquad [1.102]$$

2

DC/AC Converters

2.1. Single phase inverter and choppers

An inverter is a converter which facilitates the use of a continuous voltage source to power a load (current source) with an alternating voltage and an alternating current. The converter is therefore current- and voltage-reversible in relation to the load. This is the case of the four-quadrant chopper seen in the previous chapter. In the context of this chapter, this will be referred to as a *full bridge inverter* – single phase). The structure of the converter is shown in Figure 2.1.

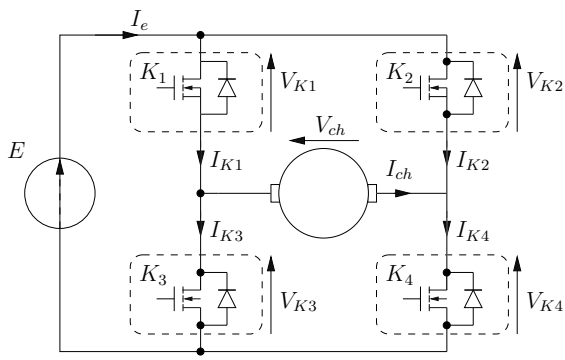


Figure 2.1. *Four-quadrant chopper = single phase full bridge inverter*

As we have seen, the chopper allows us to supply a positive or negative voltage V_{load} and current I_{load} to the load. This structure is therefore suitable for the production of an alternating voltage wave at the load terminals.

2.2. Control strategies and spectra

2.2.1. *Full wave modulation*

The notion of full wave modulation corresponds to the most basic converter control scheme. It consists of applying complementary control inputs c_a and c_b with a fixed duty cycle (equal to 50%) and frequency F_m. In this case, the voltage V_{load} at the load terminals is a square wave of frequency F_m, peak-to-peak amplitude $2E$ and an average value of zero, as seen in Figure 2.2. The Fourier series decomposition of a signal of this type (see Appendix 2) gives the following result:

$$V_{load}(t) = \sum_{p=0}^{\infty} V_{2p+1}.\sin\left(2\pi\left(2p+1\right)F_m t\right) \qquad [2.1]$$

with:

$$V_{2p+1} = \frac{4E}{\left(2p+1\right)\pi} \qquad [2.2]$$

Thus, we have a rich harmonic spectrum, so the total harmonic distortion (THD) is very high (0.435 or 0.483 depending on the definition: IEC and IEEE/DIN respectively, see Appendix 2, section A2.1.4). With these results, full wave modulation cannot be used in single phase mode, except in specific cases, i.e. in *power supplies for resonant loads*[1] (i.e. RLC circuits), as used in *induction hobs*, for example. In this

1 Due to their high filtering capacity – on the condition that the quality factor Q is high.

case, the current supplied to the load is quasi-sinusoidal, despite the fact that the voltage wave does not take this form, and the full wave modulation not only imposes a maximum amplitude for the fundamental component (peak-to-peak amplitude of $8E/\pi$), but also gives the lowest possible switching losses (two commutations per switch per period).

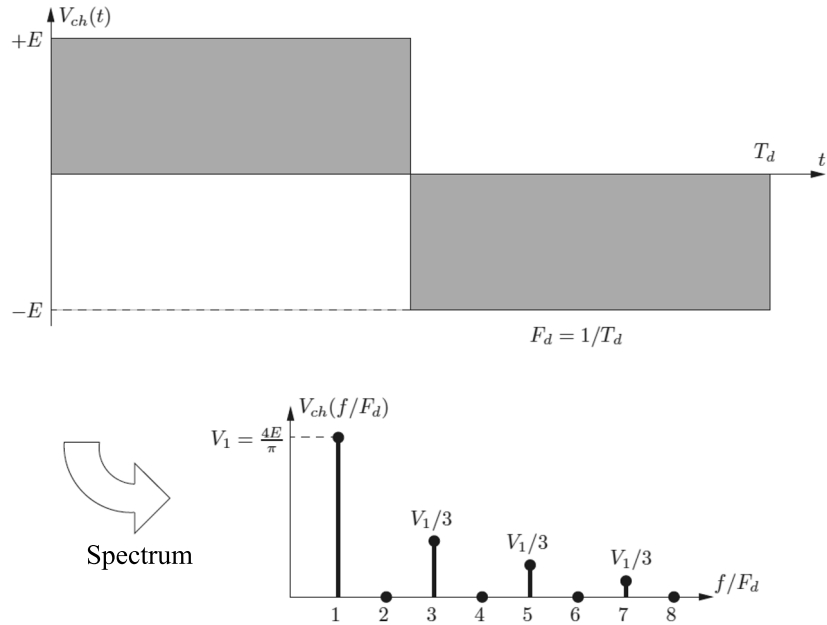


Figure 2.2. *Waveform and spectrum of the single phase full wave modulation*

THD is a synthetic performance indicator which hides the spectral description of the signal. In practice, in electrotechnics, powered loads are inductive and therefore present an impedance $\underline{Z}$ which increases as the frequency increases. If the load becomes mostly inductive, we may consider that the modulus of $\underline{Z}$ increases in a linear manner in relation to the frequency. In this case, if we wish to use the voltage power supply to deduce the quality of the current

supplied to the load, we use the notion of weighted THD. This may be considered as the THD of the current obtained for a purely inductive load (with fundamental resistance of 1Ω) powered using a given voltage. To do this, we use the fact that the current harmonics are linked to the voltage harmonics by the following relationship:

$$I_k = \frac{V_k}{k} \qquad [2.3]$$

This gives us a current THD equal to:

$$\mathrm{TDH}\,(I) = \mathrm{TDH}_{Pond/k}\,(V) = \frac{\sqrt{\sum I_k^2}}{I_1} = \frac{\sqrt{\sum \left(\frac{V_k}{k}\right)^2}}{V_1} \qquad [2.4]$$

REMARK 2.1.– This definition conforms to the IEEE/DIN standard. Adaptation to correspond to the IEC standard (see Appendix 2, section A2.1.4) with a total effective value in the denominator is problematic, as impedance can only be normalized for the fundamental. Additionally, note that this weighting is calculated for inductive loads. Other weightings (e.g. for a capacitative load) may be envisaged, but are not widely used in power electronics and electrical engineering.

2.2.2. *Intersective strategies*

So far, we have considered a bipolar strategy, for which we have shown that the average voltage $\langle V_{load} \rangle$ at the scale of the switching period T_d may be written as follows:

$$\langle V_{load} \rangle = (2\alpha - 1)\,.E \qquad [2.5]$$

where α is the duty cycle of the control signal.

The operation of this converter as an inverter simply consists of modifying the duty cycle in a sinusoidal manner (with a low modulation frequency F_m in comparison with the switching frequency $F_d = 1/T_d$). Let us take:

$$\alpha(t) = \frac{1}{2}\left(1 + K_m.\cos\left(2\pi F_m t + \varphi_m\right)\right) \qquad [2.6]$$

where φ_m is any given phase and K_m is a positive coefficient, known as the modulation, for which we can identify two cases:

– $K_m \leq 1$: *Linear modulation* of the amplitude of the "low frequency" voltage supplied to the load,

– $K_m > 1$: *Overmodulation*, where the "low frequency" voltage is no longer purely sinusoidal.

The notion of "low frequency" voltage requires spectrum analysis of the real-voltage V_{load} at the load terminals. In the case of linear modulation, we can show that, if the modulation is *synchronous* ($F_d = m.F_m$ where m is an integer), then the spectrum of this voltage includes a fundamental pulse at frequency F_m, and harmonic pulses around the "carrier" frequency F_d (pulses with frequencies F_d, $F_d - F_m$, $F_d + F_m$, $F_d - 2F_m$, $F_d + 2F_m$, etc.) and multiples of the carrier frequency ($2F_d$, $3F_d$, etc.) – see Figure 2.3(a). The analytical formulation of the Fourier series decomposition of V_{load} takes the following form:

$$V_{load}(t) = K_m E.\cos\left(2\pi F_m t + \varphi_m\right) + \sum_{p=1}^{\infty}\sum_{q=-\infty}^{\infty} V_{pq}.\cos\left(2\pi\left(p.F_d + q.F_m\right)t + \varphi_{pq}\right) \qquad [2.7]$$

In the case of overmodulation, this spectrum is modified, notably with the appearance of pulses at multiples of the modulating frequency at low frequencies ($2F_m$, $3F_m$, etc.) – see Figure 2.3(b):

$$V_{load}(t) = \sum_{k=1}^{\infty} F_k(K_m).E.\cos\left(2\pi k F_m t + \varphi_{mk}\right) + \sum_{p=1}^{\infty}\sum_{q=-\infty}^{\infty} V_{pq}.\cos\left(2\pi\left(p.F_d + q.F_m\right)t + \varphi_{pq}\right) \qquad [2.8]$$

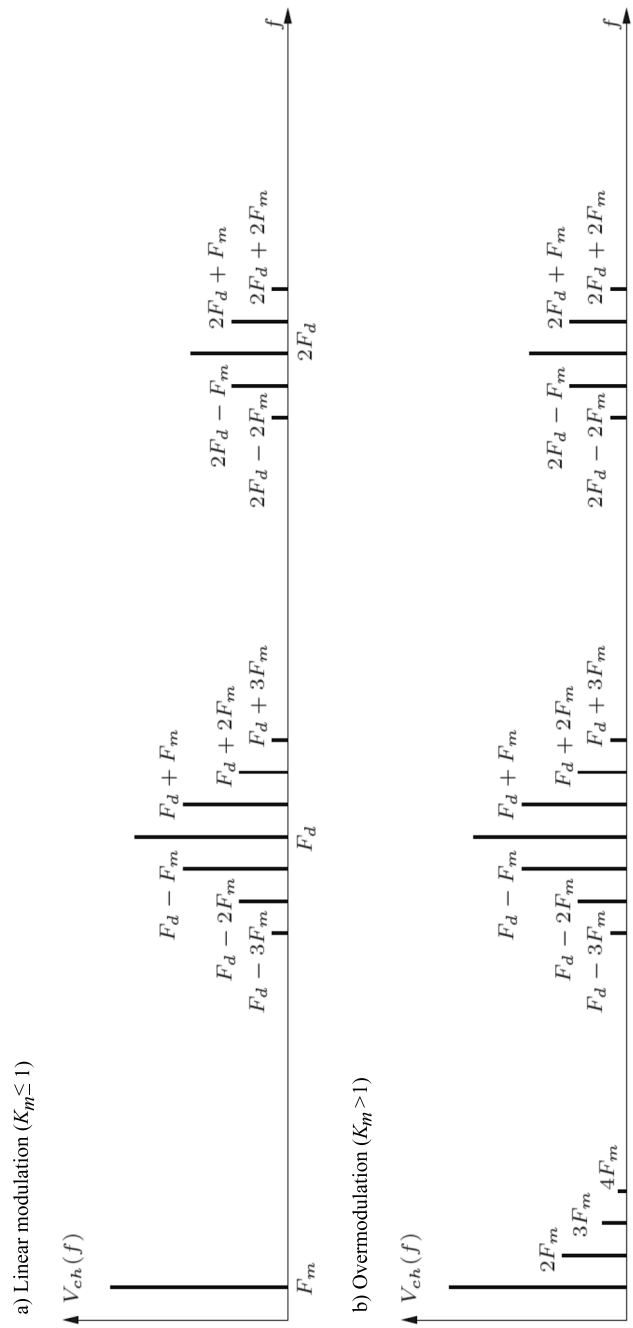


Figure 2.3. *Examples of spectra for voltage V_{load} in linear modulation and overmodulation*

Although pulses may potentially occur at the frequencies shown in Figure 2.3, the modulation strategy has an impact on the amplitude of the pulses. Figure 2.4 shows the spectrum generated by a bipolar modulation strategy and by a unipolar strategy for a fundamental of the same amplitude at frequency F_m: these graphs were obtained using Fast Fourier Transform (FFT) in a calculation program (Matlab/Simulink) for a power voltage $E = 100$ V, a switching frequency $F_d = 2$ kHz and a modulation frequency $F_m = 100$ Hz. As the modulation index K_m is fixed at 0.8, the amplitude of the fundamental at 100 Hz is 80 V.

The principle of unipolar modulation involves only modulating the control of one half-bridge at a time. Thus, when we wish to produce a positive voltage, the half-bridge (K_2, K_4) is switched to position $c_b = 0$ (modulating c_a); for a negative output voltage, half-bridge (K_1, K_3) is switched to state $c_a = 0$ (modulating c_b).

In concrete terms, to create a strategy of this type, intersective PWM is used (see Appendix 1), for which we use two triangular, unipolar and opposite sub-carriers (varying between 0 and $+P_{max}$ for switching function c_a and between $-P_{max}$ and 0 for switching function c_b). An illustration of this control scheme is shown in Figure 2.5.

REMARK 2.2.– Another solution may be used: for positive switching, we put (K_1, K_3) into state $c_a = 1$ (modulating c_b), and for negative switching, we put (K_2, K_4) into state $c_b = 1$ (modulating c_a). In reality, a combination of the two solutions is preferable in order to balance the use of switches and thus balance losses (both through conduction and switching).

The waveforms obtained take values of $+E$, 0 and $-E$, unlike bipolar PWM, where only values $+E$ and $-E$ are accessible. There are no direct "edges" between $+E$ and $-E$, reducing the amplitude of high frequency (HF) harmonics.

This can be seen in Figure 2.4 in the pulses around the carrier frequency (2 kHz); in bipolar PWM, the level of the most significant pulse (at 2 kHz) is close to that of the fundamental component at 100 Hz (80 V), whereas in unipolar PWM, the largest pulses are located at $F_p - F_m$ =1,900 Hz and $F_p + F_m$ =2,100 Hz with a lower amplitude.

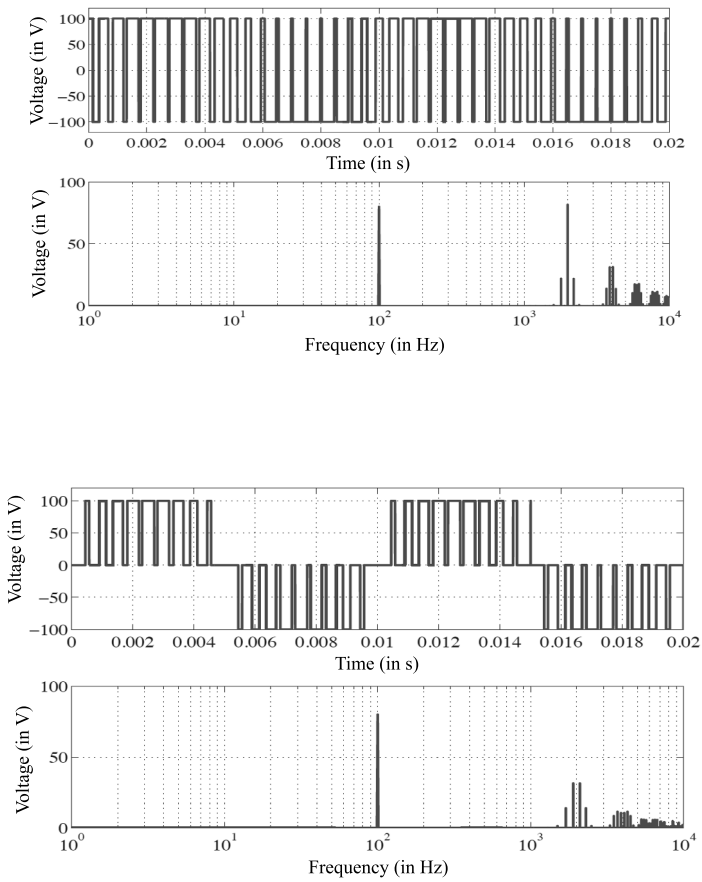


Figure 2.4. *Spectra obtained using simulation for bipolar a) and unipolar b) modulation*

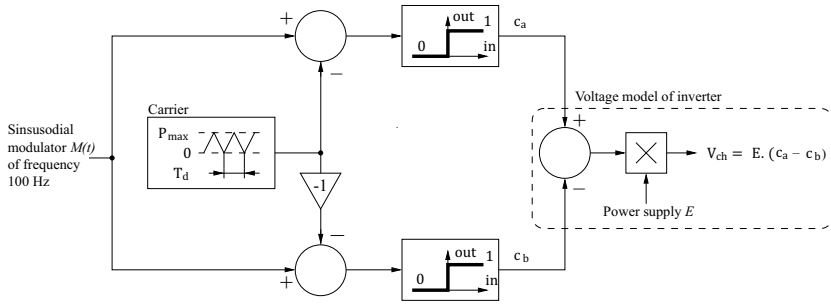


Figure 2.5. *Structure of a "unipolar" PWM controller*

These spectral aspects may appear to be irrelevant due to the fact that currents will be filtered by the load, which is inductive in nature. In cases with a high difference between the chopping frequency F_d and the modulating frequency F_m, it is not possible for voltage harmonics to induce high current harmonics. However, these electromagnetic disturbance aspects should be taken into account, as even weak disturbances in terms of amplitude can cause failures in neighboring equipment, or even self-disturbance within the converter (particularly in the control structure). Finally, note that single-phase inverters are not designed to power machines (which are generally three-phase in the case of alternating current machines[2]), but rather for use in uninterruptible power supplies (UPS). In this context, they are generally used with LC filters in order to generate sinusoidal instantaneous voltages. Consequently, the spectral content of the voltage wave has a direct impact on the quality of the output voltage of the UPS (better quality for unipolar PWM) for a given filter, or will have an impact on the dimensioning of the filter for a given output voltage quality (requiring a larger, and thus more costly, filter in the case of bipolar PWM).

2 Single-phase AC machines do exist (for example asynchronous auxiliary winding/capacitor machines or shaded-pole motors), but these are directly integrated into the network and are rarely associated with a converter.

2.2.3. *Precalculated PWM*

2.2.3.1. *General points*

So far, we have considered full wave modulation and intersective PWM. Full wave modulation presents the advantage of reducing switching losses (in addition to a high fundamental amplitude) to the detriment of the THD (weighted) of the waveform. Intersective PWMs, on the other hand, produce waves of high quality in terms of THD, but with much higher switching losses (increased by an order of around F_d/F_m). Moreover, the amplitude of the fundamental is reduced in linear modulation mode to 21.5% of that obtained using full wave mode. Nevertheless, overmodulation remains possible, and allows us to tend toward full wave modulation for $K_m \gg 1$ (with a weighted TDH during periods of increase). However, the problem of switching losses remains, and at very high powers (for example for rail traction), these values may be incompatible with the use of intersective PWM. As we have seen, intersective PWM requires a high F_d/F_m ratio in order to avoid the emergence of parasitic sub-harmonic pulses, similar to aliasing, which are problematic in sampled systems (see Appendix 2).

Based on this observation, a solution situated somewhere between full wave modulation and intersective PWM would be ideal. The use of microprocessors and digital control allows us to envisage control strategies which would not have been possible using analog electronics alone. A compromise has been identified in the form of precalculated PWM, where we aim to obtain the best possible weighted THD with a limited number of commutations per switch and per fundamental period. For example, instead of the two effective commutations in full wave modulation, we might choose to produce a voltage wage with four, six or eight commutations per fundamental period. The gain in terms of the number of degrees of freedom should then be exploited in order to cancel out certain harmonics in the waveform (those with the lowest

frequencies), or to attenuate all of the harmonics present in a given frequency range. However, this solution comes at a price: the equations to solve are complex (as they are nonlinear), and are thus impossible to solve in real-time using the converter control element. Switching instants must therefore be calculated offline and memorized (hence the term "precalculated") then reproduced by the controller during use. Therefore, this method does not offer the same flexibility as intersective (or natural) PWM, and sequence sets need to be tabulated in a memory element integrated into the controller [LAN 09].

We will not provide an exhaustive examination of this subject here; instead, we will focus on harmonic cancellation for a bipolar waveform such as that shown in Figure 2.6. The figure shows a signal with 10 commutations per period, parameterized using two switching angles, α_1 and α_2.

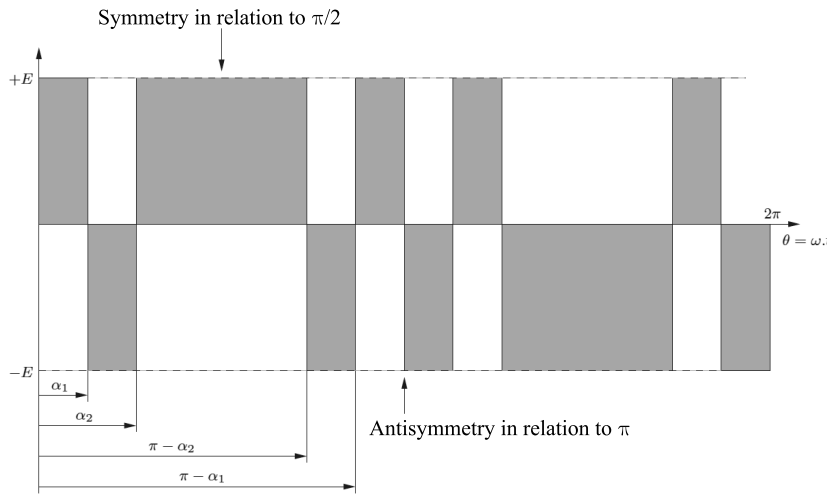


Figure 2.6. *Composition of a waveform for precalculated PWM*

2.2.3.2. *Fourier series decomposition*

The Fourier series decomposition of the 2π-periodic signal $x(\theta)$ defined in Figure 2.6 may be established using the

definitions given in Appendix 2. However, in this section, we wish to begin by highlighting the symmetrical aspects of the signal in order to simplify our study:

– the signal has an average value of zero, hence $a_0 = 0$;

– we note that the signal is odd when described over a full period $[0; 2\pi]$, implying that $\forall k \in \mathbb{N},\ a_k = 0$;

– finally, note that a "sliding symmetry" exists (antisymmetric to $\theta = \pi$, i.e. in the middle of the period), which implies that $\forall k \in \mathbb{N},\ b_{2k} = 0$.

Consequently, only the odd harmonics b_{2k+1} are non-null. We can therefore focus on these coefficients, expressed as:

$$b_{2k+1} = \frac{8}{2\pi} \int_0^{\pi/2} x(\theta).\sin\left((2k+1)\,\theta\right).d\theta \qquad [2.9]$$

This integral may be split into three terms, following the evolution of $x(t)$ in this interval:

$$b_{2k+1} = \frac{8E}{2\pi} \left(\int_0^{\alpha_1} \sin\left((2k+1)\,\theta\right).d\theta - \int_{\alpha_1}^{\alpha_2} \sin\left((2k+1)\,\theta\right).d\theta + \int_{\alpha_2}^{\pi/2} \sin\left((2k+1)\,\theta\right).d\theta \right) \qquad [2.10]$$

Integration is then easy to carry out, and we obtain:

$$b_{2k+1} = \frac{4E}{\pi} \left(\frac{1 - 2\cos\left((2k+1)\,\alpha_1\right) + 2\cos\left((2k+1)\,\alpha_2\right)}{2k+1} \right) \qquad [2.11]$$

With the two parameters α_1 and α_2, we then hope to cancel out two components (for example b_3 and b_5) using the following system:

$$\begin{cases} b_3 = \frac{4E}{\pi} \left(\frac{1 - 2\cos(3\alpha_1) + 2\cos(3\alpha_2)}{3} \right) = 0 \\ b_5 = \frac{4E}{\pi} \left(\frac{1 - 2\cos(5\alpha_1) + 2\cos(5\alpha_2)}{5} \right) = 0 \end{cases} \qquad [2.12]$$

While these equations are simple to formulate, their solution is complex and cannot be envisaged in real-time. Moreover, we should remember that we wish to control the amplitude of the fundamental; in this case, we cannot simply use the two degrees of freedom to cancel out harmonics. We also need to consider the control of b_1, fixed at a reference value b_1^{ref}:

$$b_1 = \frac{4E}{\pi}\left(1 - 2\cos\left(\alpha_1\right) + 2\cos\left(\alpha_2\right)\right) = b_1^{ref} \qquad [2.13]$$

In fact, if we take $\alpha_1 = 23.6°$ and $\alpha_2 = 33.3°$, we cancel out b_3 and b_5, but this imposes $b_1 = 1,068 \times E$. The spectrum of the signal obtained for these values of α_1 and α_2 is shown in Figure 2.7 for reference purposes.

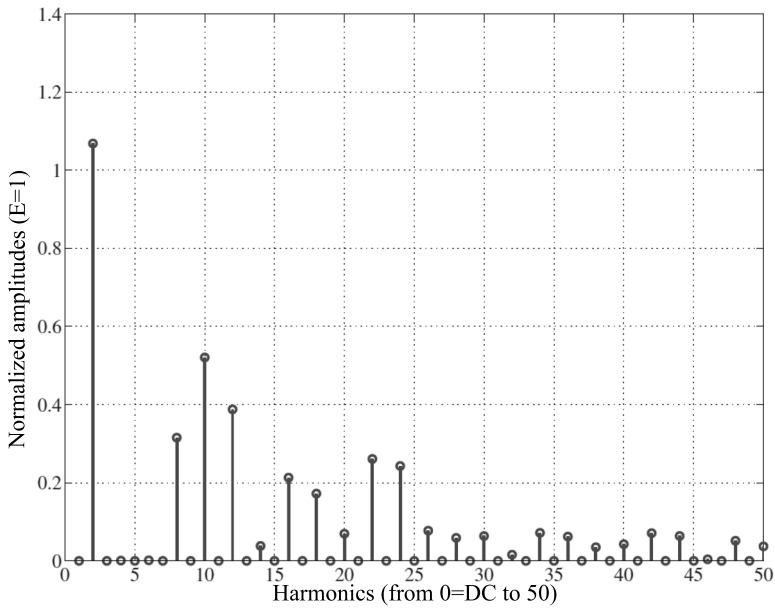


Figure 2.7. *Spectrum of the PWM signal from Figure 2.6 for* $\alpha_1 = 23.6°$ *and* $\alpha_2 = 33.3°$

2.3. "Value" half-bridge inverters

The economic aspects of converter design may lead us to consider a simplified structure of the single-phase inverter. If we consider a two-quadrant current-reversible chopper, used in PWM inverter mode, we note that the modulation of the duty cycle $\alpha(t)$ allows us to produce an average voltage $\langle V_s \rangle$[3] between the midpoint (point separating the two switches) and the negative terminal of the source E (known as the "mass"), of the form:

$$\langle V_s \rangle = \frac{E}{2} \left(1 + K_m . \cos\left(2\pi F_m t + \varphi_m\right)\right) \qquad [2.14]$$

for:

$$\alpha = 1/2 . \left(1 + K_m . \cos\left(2\pi F_m t + \varphi_m\right)\right) \qquad [2.15]$$

Here, the linear modulation range is still $K_m \leq 1$. This "low frequency" voltage is purely sinusoidal for a sinusoidal modulation within this range, but if K_m exceeds 1, then "low frequency" harmonics will appear at frequencies $2F_m$, $3F_m$, etc.

To obtain the desired result, we still need to eliminate the continuous component $E/2$. To do this, we must simply "plug in" the powered load between the midpoint of the half-bridge and the midpoint of a series assembly of two identical voltage sources with a value of $E/2$, as shown in the diagram in Figure 2.8(a).

In practice, we do not always have access to a midpoint power supply such as that shown above, but simply to a source E. In this case, it is possible to artificially create two

3 Once again, this is a sliding average within the switching period, evolving slowly at the frequency F_m of the sinusoidal modulation signal acting on the duty ratio.

half-sources with a value $E/2$ by including a capacitance bridge, created using two identical capacitors, for which we must determine a capacity C_0 (Figure 2.8(b)). A capacitance bridge of this type powered by source E may be modeled as an equivalent Thévenin source (E_{th}, Z_{th}), for which we obtain:

$$E_{th} = \frac{E}{2} \qquad [2.16]$$

and:

$$Z_{th} = \frac{1}{j2C_0\omega} \qquad [2.17]$$

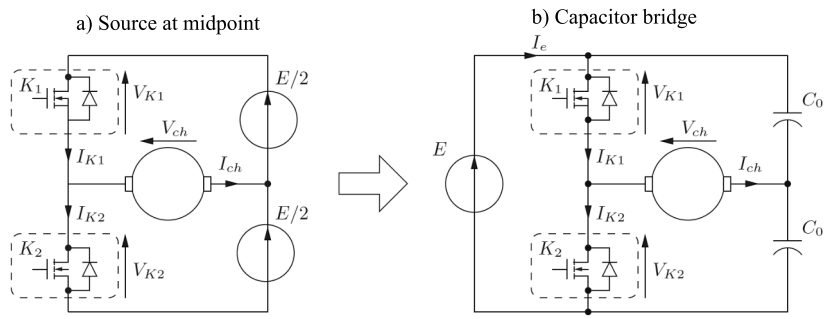


Figure 2.8. *Half-bridge single phase inverter*

This gives us a voltage source with a value of $E/2$ (as required), but which presents an impedance equivalent to that of a capacitor with capacity $2C_0$. In practice, we must ensure that the impedance of this equivalent capacitor is low in relation to that of the powered load, in order for the inverter to operate in the required manner. This may impose significant limitations if we wish to power a load with a very low frequency, as, unless it is significantly over-dimensioned, the capacitor will present a very high impedance value. In this situation, a full bridge inverter, as described in the previous section, would be preferable, despite doubling the number of transistors and diodes required.

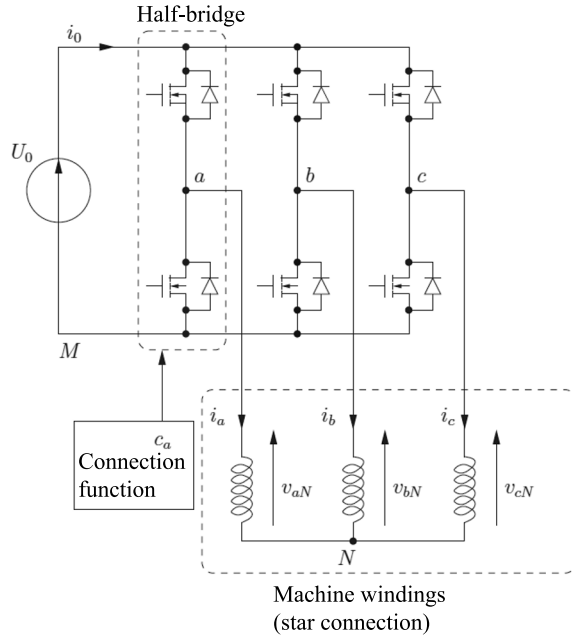


Figure 2.9. *Three-phase voltage inverter*

2.4. Three-phase inverter

2.4.1. *Structure and modeling*

The structure of the three-phase inverter is a simple extension of the full-bridge chopper using three half-bridges, as shown in Figure 2.9. It would be possible to create a converter using three full-bridge single-phase inverters (giving us 12 switches, each made up of a transistor and a diode), but this "luxury" solution is superfluous in the case of a load with only three connections (known as "phases"). This is the most widespread configuration, as, although most machines have a connection block with six accessible terminals (two per phase); these terminals are connected *in situ* following a star or triangle layout (see Figure 2.10), leaving three connections accessible to the user.

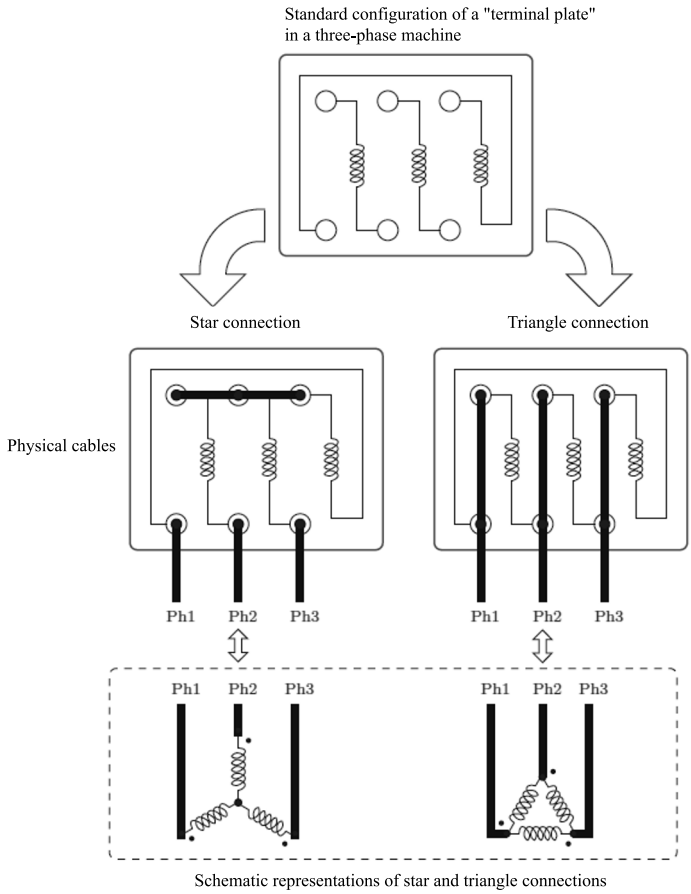


Figure 2.10. *Triangle and star connections in electrical machines*

This choice was made because it is pointless to input a current system with a sum other than zero (this sum is known as a “zero sequence current”) into a symmetric and balanced machine, as this zero sequence component presents no advantages in terms of electromechanical conversion; in other terms, the current generates no mechanical connections within the machine. As long as we do not wish to inject a current of this type into the windings of a machine, then

there is no need for three separate converters; the three-phase inverter with three half-bridges may be seen as the most simplified version of this structure.

In the context of this study, we can therefore assume that the sum of the currents injected into the phases of the machine is null:

$$i_a + i_b + i_c = 0 \qquad [2.18]$$

We also consider that this is balanced in electrical modeling terms (each phase has the same impedance – R_s, L_s – and e.m.f. values e_a, e_b and e_c also constitute a balanced three-phase system: $e_a + e_b + e_c = 0$). We can therefore write:

$$v_{aN} + v_{bN} + v_{cN} = 0 \qquad [2.19]$$

Using this basis, we will now attempt to express the voltages v_{xN} applied to the phases of the machine ($x \in \{a, b, c\}$) as a function of the power voltage U_0 of the inverter and the switching functions c_x associated with each half-bridge.

To simplify the written expression of these equations, we will use a matrix formulation, using the following vectors (noted in bold):

– $\mathbf{v}_{3N} = (v_{aN}, v_{bN}, v_{cN})^t$;

– $\mathbf{v}_{3M} = (v_{aM}, v_{bM}, v_{cM})^t$;

– $\mathbf{c}_3 = (c_a, c_b, c_c)^t$;

– $\mathbf{i}_3 = (i_a, i_b, i_c)^t$.

As in the case of the current reversible two quadrant chopper, we may write that:

$$\forall x \in \{a, b, c\}, \quad v_{xM} = U_0.c_x \qquad [2.20]$$

In matrix form, this gives us:

$$\mathbf{v}_{3M} = U_0.\mathbf{c}_3 \qquad [2.21]$$

Using the loop law, we can easily demonstrate that the line-to-line voltages u_{ij} with $i, j \in \{a, b, c\}$ may be written as:

$$u_{ij} = v_{iM} - v_{jM} = U_0.\,(c_i - c_j) \qquad [2.22]$$

but also:

$$u_{ij} = v_{iN} - v_{jN} \qquad [2.23]$$

These final two equalities give us the following matrix equation:

$$\underbrace{\begin{pmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{pmatrix}}_{M}.\mathbf{v}_{3N} = U_0.\begin{pmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{pmatrix}.\mathbf{c}_3 \qquad [2.24]$$

This system, with three equations and three unknown variables (v_{aN}, v_{bN} and v_{cN}) cannot be solved directly, as matrix M is not invertible. By applying Sarrus rule, we can easily verify that:

$$\det(M) = 0 \qquad [2.25]$$

However, by replacing one of the equations in the system with equation [2.19], we obtain the following matrix equation:

$$\underbrace{\begin{pmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{pmatrix}}_{M'}.\mathbf{v}_{3N} = U_0.\begin{pmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 0 & 0 & 0 \end{pmatrix}.\mathbf{c}_3 \qquad [2.26]$$

where M' is now an invertible matrix. This allows us to obtain the desired relationship, i.e.:

$$\mathbf{v}_{3N} = U_0.\begin{pmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 1 & 1 & 1 \end{pmatrix}^{-1} \cdot \begin{pmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ 0 & 0 & 0 \end{pmatrix}.\mathbf{c}_3$$

$$= \frac{U_0}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}.\mathbf{c}_3 \qquad [2.27]$$

This model can only be considered complete if a relationship is established connecting currents i_a, i_b, i_c and i_0. We note that the instantaneous input p_e and output p_s power values from the converter are identical, given that the converter is presumed to be ideal (i.e. not subject to losses) and that it does not include any energy storage components (inductances or capacitors). We may therefore take the following expressions of p_e and p_s:

$$\begin{cases} p_e = U_0.i_0 \\ p_s = \mathbf{v}_{3N}^t.\mathbf{i}_3 \end{cases} \qquad [2.28]$$

thus, taking $p_e = p_s$, we obtain:

$$i_0 = \frac{1}{3}\mathbf{c}_3^t.\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}.\mathbf{i}_3 \qquad [2.29]$$

REMARK 2.3.– To obtain this result, we must take account of the following property of the transposition of a matrix product:

$$\begin{cases} (A.B)^t = B^t.A^t \\ (A.B.C)^t = C^t.B^t.A^t \end{cases} \qquad [2.30]$$

2.4.2. *Modulation by intersective PWM*

The application of intersective PWM to the control of three-phase inverters involves generalizing the technique used for the single-phase inverter and the current-reversible two quadrant chopper: an additional control input is applied for the switches on one supplementary half-bridge. As in the case of the single-phase inverter, we then define the duty ratio α_x associated with half-bridge x as the average value of the connection function c_x. We can then produce the expression of the "low frequency" voltages $\langle v_{xN} \rangle$ supplied to the load. The vector of these "average" voltages is simply noted $\langle \mathbf{v}_{3N} \rangle$. In the same way, we take α_3 to be the vector of the duty ratios α_a, α_b and α_c. Then, we can write:

$$\langle \mathbf{v}_{3N} \rangle = \underbrace{\frac{U_0}{3} \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}}_{G} . \alpha_3 \qquad [2.31]$$

The simplest form of modulation consists of applying three sinusoidal duty ratios, with a shift of 120°:

$$\begin{cases} \alpha_a(t) = 1/2.(1 + K_m.\cos(2\pi F_m t)) \\ \alpha_b(t) = 1/2.(1 + K_m.\cos(2\pi F_m t - 2\pi/3)) \\ \alpha_c(t) = 1/2.(1 + K_m.\cos(2\pi F_m t + 2\pi/3)) \end{cases} \qquad [2.32]$$

where F_m is the modulation frequency (as for other types of converters, let F_d be the switching frequency such that $F_d \gg F_m$) and K_m is the depth of modulation, defined as in the case of the single-phase inverter, i.e. $K_m \leq 1$ for a linear modulation and $K_m > 1$ for overmodulation. The matrix formulation of vector α_3 gives us:

$$\alpha_3 = \underbrace{\frac{1}{2}\begin{pmatrix}1\\1\\1\end{pmatrix}}_{C_{31}} + \frac{K_m}{2}\begin{pmatrix}\cos(2\pi F_m t)\\ \cos(2\pi F_m t - 2\pi/3)\\ \cos(2\pi F_m t + 2\pi/3)\end{pmatrix} \quad [2.33]$$

The first term in this expression is known as the zero sequence component (linked to matrix C_{31}); the second term has components with a zero sum, and may be reformulated using a "cos/sin" two phase decomposition. To do this, we simply note that:

$$\begin{pmatrix}\cos(2\pi F_m t)\\ \cos(2\pi F_m t - 2\pi/3)\\ \cos(2\pi F_m t + 2\pi/3)\end{pmatrix} = \underbrace{\begin{pmatrix}1 & 0\\ -1/2 & \sqrt{3}/2\\ -1/2 & -\sqrt{3}/2\end{pmatrix}}_{C_{32}} . \begin{pmatrix}\cos(2\pi F_m t)\\ \sin(2\pi F_m t)\end{pmatrix} \quad [2.34]$$

The association of matrix C_{31} and matrix C_{32} is known as the "Clarke transform" (named after its inventor, Edith Clarke), and connects any given three-phase vector $\mathbf{x}_3$ to the couple $\mathbf{x}_2 = (x_\alpha, x_\beta)^t$ (two-phase vector), x_0 (zero sequence – scalar):

$$\mathbf{x}_3 \stackrel{\Delta}{=} C_{32}.\mathbf{x}_2 + C_{31}.x_0 \quad [2.35]$$

REMARK 2.4.– Matrices C_{31} and C_{32} present a number of key properties, given as:

$$C_{31}^t C_{31} = 3 \quad [2.36]$$

$$C_{32}^t C_{32} = \underbrace{\frac{3}{2}\begin{pmatrix}1&0\\0&1\end{pmatrix}}_{\mathbb{I}_2} \quad [2.37]$$

$$C_{31}^t C_{32} = \begin{pmatrix} 0 & 0 \end{pmatrix} \quad [2.38]$$

$$C_{32}^t C_{31} = \begin{pmatrix} 0 \\ 0 \end{pmatrix} \quad [2.39]$$

This transform is useful due to a notable property of the gain matrix G of the inverter:

$$G = \frac{2U_0}{3} C_{32} C_{32}^t \quad [2.40]$$

Having established this property, we can immediately use it to simplify equation [2.31]:

$$\begin{aligned} \langle \mathbf{v}_{3N} \rangle &= \tfrac{2U_0}{3} C_{32} C_{32}^t . \left(\tfrac{1}{2} C_{31} + \tfrac{K_m}{2} C_{32} . \begin{pmatrix} \cos(2\pi F_m t) \\ \sin(2\pi F_m t) \end{pmatrix} \right) \\ &= \tfrac{K_m U_0}{2} C_{32} . \begin{pmatrix} \cos(2\pi F_m t) \\ \sin(2\pi F_m t) \end{pmatrix} \end{aligned} \quad [2.41]$$

In this way, we show that the "low frequency" line-to-neutral voltages $\langle v_{xN} \rangle$ applied to the load are effectively sinusoidal, with frequency F_m and amplitude $K_m.U_0/2$ (so with a maximum of $U_0/2$ for a linear modulation) and form a balanced three-phase system.

The waveform of a line-to-neutral voltage is shown in Figure 2.11 for the case of a sinusoidal modulation with frequency $F_m = 100\,\text{Hz}$ with a carrier frequency $F_d = 2\,\text{kHz}$, modulation depth $K_m = 0.8$ and a DC bus voltage $U_0 = 100\,\text{V}$. The corresponding spectrum is shown in Figure 2.12.

We see that the low frequency content of the spectrum is limited to a single pulse at 100 Hz, whilst pulses also occur around the carrier frequency and its multiples, as in the case of the single-phase inverter. Considering the waveform, we

see that three instantaneous values are available: $(-2U_0/3, -U_0/3, 0, U_0/3, 2U_0/3)$.

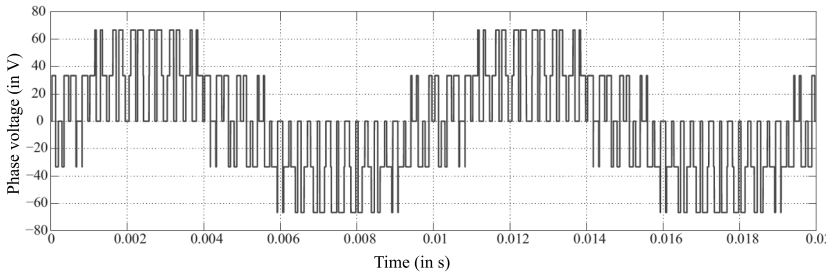


Figure 2.11. *Waveform of a line-to-neutral voltage for intersective sinusoidal PWM (bipolar)*

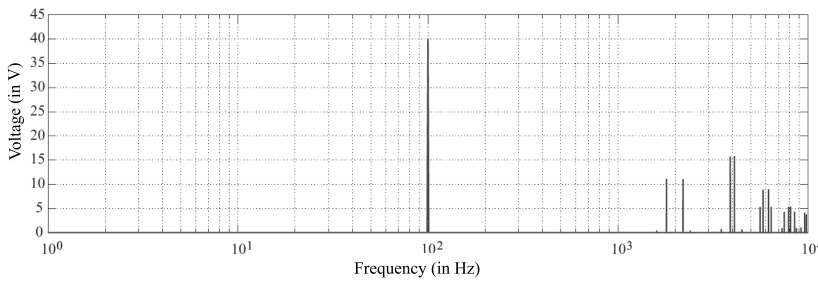


Figure 2.12. *Spectrum of a line-to-neutral voltage for intersective sinusoidal PWM*

2.4.3. *"Full wave" modulation*

Full wave modulation for a three-phase inverter uses the same techniques as for a single-phase inverter, where the half-bridge connection function is kept at 1 for half a period $T_m/2$ (where $T_m = 1/F_m$) and at 0 for the following half-period. This technique may be adapted for a three-phase inverter by simply shifting the switching functions of the half-bridges, taken by pairs, by a third of a period (i.e. by 120°) as shown in Figure 2.13.

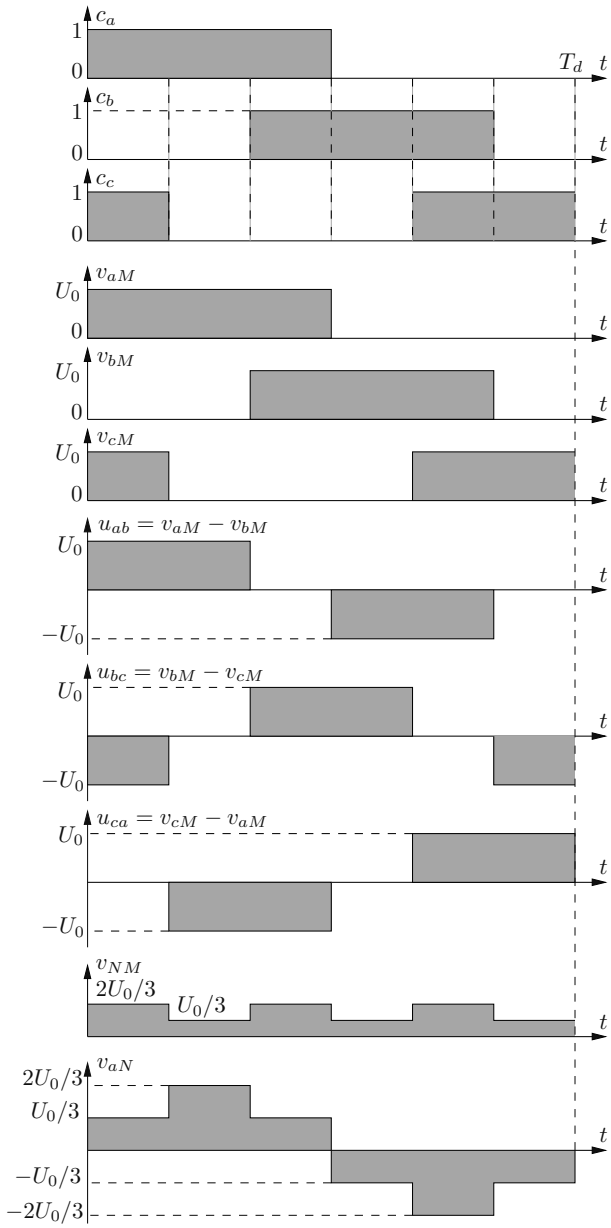


Figure 2.13. *Control signals and voltages in full wave modulation*

We see that the line-to-line voltages present visible sequences of the form $-U_0$, 0, $+U_0$ and 0. These states are maintained for periods of $T_d/3$, $T_d/6$, $T_d/3$ and $T_d/6$ respectively. Therefore, the Fourier series decomposition of voltage u_{ab} is as follows:

$$u_{ab} = \sum_{p=0}^{\infty} U_{2p+1}.\sin\left(2\pi\left(2p+1\right)F_m t\right) \qquad [2.42]$$

with:

$$U_{2p+1} = \frac{4U_0}{\left(2p+1\right)\pi}\cos\left(\frac{\left(2p+1\right)\pi}{6}\right) \qquad [2.43]$$

In this expression, we see that the spectrum contains not only odd harmonics (the usual result), but that all harmonics which are multiples of 3 have an amplitude of zero (harmonics 3, 9, 15, etc). Once we have obtained the line-to-line voltage spectrum, we can also determine the spectrum of the line-to-neutral voltages.

If we simply wish to determine the amplitude V_{fond} of the fundamental of the line-to-neutral voltages, we simply obtain:

$$V_{fond} = \frac{2U_0}{\pi} \qquad [2.44]$$

This amplitude should be compared to that accessible without distortion with a sinusoidal intersective PWM, which is equal to $U_0/2$ (result established in the previous section). "Full wave" modulation therefore produces a gain of over 27%. However, in the next section, covering vector PWM, we will show that another solution offers even better performances from this perspective, while conserving a purely sinusoidal "low frequency" waveform. Full wave modulation still produces the highest possible amplitude, but to the detriment of spectrum quality.

An important point in full wave operation lies in the fact that at the three switching functions are never in the same state at the same moment (whether 0 or 1). When the combinations $c_a = c_b = c_c = 0$ or $c_a = c_b = c_c = 1$ occur, we see that the instantaneous line-to-neutral voltage vector $\mathbf{v}_{3N}$ is null. In full wave modulation, we systematically avoid application of this null vector, a fact which explains the fact that the voltage wave has a maximum amplitude. As we have three binary control variables, we have $2^3 = 8$ possible combinations for controlling the full inverter. As we have seen that two of these configurations are never used, full wave modulation only uses six control combinations. This corresponds to the six voltage levels identified in the line-to-neutral voltages shown in Figure 2.13. This fact is reflected in the alternative name for the technique, which is also known as *six-step modulation*.

2.4.4. *Vector PWM modulation*

The last approach which we will discuss here is based on the use of the Clarke transform, as defined in equation [2.35], and the factorization of the gain matrix G of the inverter. Rather than considering the line-to-neutral voltages $\mathbf{v}_{3N}$ supplied to the load, we will consider the equivalent two-phase vector $\mathbf{v}_{2N}$, as we know that the zero sequence component of $\mathbf{v}_{3N}$ is null (as we have a balanced three-phase system):

$$\mathbf{v}_{3N} = C_{32}.\mathbf{v}_{2N} = \frac{2U_0}{3} C_{32}.C_{32}^t.\mathbf{c}_3 \qquad [2.45]$$

After simplification (by "left side" multiplication of both elements by C_{32}^t), we obtain:

$$\mathbf{v}_{2N} = \frac{2U_0}{3}.C_{32}^t.\mathbf{c}_3 \qquad [2.46]$$

The list of possible values (components v_α and v_β of $\mathbf{v}_{2N}$) is shown in Table 2.1 and these results are illustrated by the constellation of corresponding vectors in Figure 2.14. We wish to produce a voltage vector $\mathbf{v}_{2N}^{ref}$ (setpoint) located in the two-phase plane (as an average value, for a switching period T_d). This vector must also lie within the hexagon formed by connecting the extremities of vectors $\mathbf{V}_1$ to $\mathbf{V}_6$ to enable the inverter to function in linear mode. This setpoint vector may be localized according to the sector (i) in which it is found, as shown in the figure.

Vector PWM consists of projecting the setpoint vector (which is generally not instantly accessible) following two base vectors. This decomposition is carried out following the two vectors delimiting sector (i), which is determined in advance. We therefore wish to write $\mathbf{v}_{2N}^{ref}$ in the form:

$$\mathbf{v}_{2N}^{ref} = \lambda_i.\mathbf{V}_i + \lambda_{i+1}.\mathbf{V}_{i+1} \qquad [2.47]$$

Control (c_a, c_b, c_c)	v_α/U_0	v_β/U_0	*Vector name*
$(0,0,0)$	0	0	$\mathbf{V}_0$
$(1,0,0)$	$2/3$	0	$\mathbf{V}_1$
$(1,1,0)$	$1/3$	$1/\sqrt{3}$	$\mathbf{V}_2$
$(0,1,0)$	$-1/3$	$1/\sqrt{3}$	$\mathbf{V}_3$
$(0,1,1)$	$-2/3$	0	$\mathbf{V}_4$
$(0,0,1)$	$-1/3$	$-1/\sqrt{3}$	$\mathbf{V}_5$
$(1,0,1)$	$1/3$	$-1/\sqrt{3}$	$\mathbf{V}_6$
$(1,1,1)$	0	0	$\mathbf{V}_7 = \mathbf{V}_0$

Table 2.1. *Voltage values* $v_{2N} = (v_\alpha, v_\beta)^t$ *available for all control combinations* (c_a, c_b, c_c)

REMARK 2.5.– Indexes i and $i+1$ are defined as "modulo 6". Thus, in the case where $\mathbf{v}_{2N}^{ref}$ is located in sector (6), we take $i = 6$ and $i + 1 = 7 \rightarrow 1$.

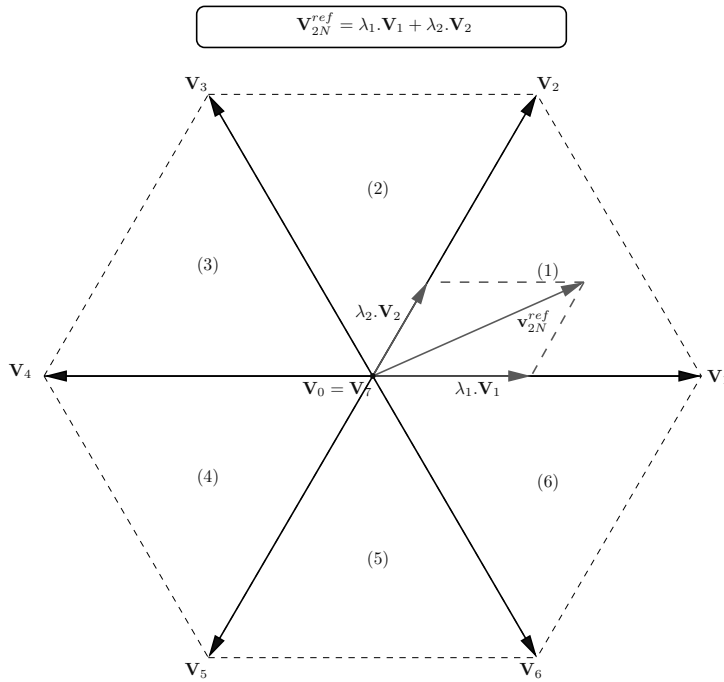


Figure 2.14. *Constellation of instant vectors* $\mathbf{v}_{2N}$ *available as inverter output. For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

Before calculating the coordinates λ_i and λ_{i+1} of the vector (v_{2s}), we need to decompose angle α (as shown in Figure 2.14 with an example of vector $\mathbf{v}_{2N}^{ref}$ for $i = 1$):

$$\alpha = \frac{(i-1)\,\pi}{3} + \widetilde{\alpha} \qquad [2.48]$$

We can thus give the expression of vector $(\mathbf{v}_{2s})$ by replacing α with this expression:

$$\mathbf{v}_{2N}^{ref} = V \cdot P\left(\frac{(i-1)\,\pi}{3} + \widetilde{\alpha}\right) \cdot \begin{pmatrix} 1 \\ 0 \end{pmatrix} \qquad [2.49]$$

where $P(\cdot)$ is the 2D rotation matrix, defined as follows:

$$P(\varphi) = \begin{pmatrix} \cos\varphi & -\sin\varphi \\ \sin\varphi & \cos\varphi \end{pmatrix} \quad [2.50]$$

Thus, we can identify the two expressions [2.47] and [2.49] in order to establish two equations with two unknown variables (λ_i and λ_{i+1}):

$$\begin{cases} \lambda_i + \frac{\lambda_{i+1}}{2} = \frac{V}{\frac{2U_0}{3}} \cdot \cos\widetilde{\alpha} \\ \frac{\sqrt{3}}{2} \cdot \lambda_{i+1} = \frac{V}{\frac{2U_0}{3}} \cdot \sin\widetilde{\alpha} \end{cases} \quad [2.51]$$

This system may be written in the form $W.\Lambda = X$, where $\Lambda = (\lambda_i, \lambda_{i+1})^t$ with:

$$W = \begin{pmatrix} 1 & 1/2 \\ 0 & \sqrt{3}/2 \end{pmatrix}$$

$$\text{and} \qquad X = \frac{V}{\frac{2U_0}{3}} \cdot \begin{pmatrix} \sin\left(\frac{\pi}{3} - \widetilde{\alpha}\right) \\ \sin\widetilde{\alpha} \end{pmatrix}$$

The solution is therefore written as:

$$\Lambda = W^{-1}.X = \frac{V}{U_0} \cdot \begin{pmatrix} \sin\left(\frac{\pi}{3} - \widetilde{\alpha}\right) \\ \sin\widetilde{\alpha} \end{pmatrix} \quad [2.52]$$

REMARK 2.6.– We note that coordinates $(\lambda_i, \lambda_{i+1})^t$ are dimensionless.

Decomposition using the vectors delimiting sector (i) is not the only possible method. If we consider the example of vector $\mathbf{v}_{2N}^{ref}$, we see that this cannot only be decomposed using $\mathbf{V}_2$ and $\mathbf{V}_3$, but also using $\mathbf{V}_2$ and $\mathbf{V}_4$ or $\mathbf{V_1}$ and $\mathbf{V}_3$.

These coordinates will be used in the final stage for the creation of control sequences. Each coordinate represents the

fraction of the switching period during which the corresponding base vector must be maintained.

2.4.4.1. *Sequence creation*

2.4.4.1.1. Duration of sequence phases

In the previous section, we identified the coordinates λ_i and λ_{i+1} associated with the base vectors $\mathbf{V}_i$ and $\mathbf{V}_{i+1}$ which will be applied during part of the switching period T_d.

Thus, vector $\mathbf{V}_i$ is applied for a duration τ_i defined by the relationship:

$$\tau_i = \lambda_i.T_d \qquad [2.53]$$

In the same way, we obtain the duration of application τ_{i+1} of vector $\mathbf{V}_{i+1}$, defined as:

$$\tau_{i+1} = \lambda_{i+1}.T_d \qquad [2.54]$$

Taken together, these durations cannot exceed T_d. This gives us the following inequality for components λ_i and λ_{i+1}:

$$\lambda_i \ + \lambda_{i+1} \leq 1 \qquad [2.55]$$

The last fraction of T_d, not used by the two vectors $\mathbf{V}_i$ and $\mathbf{V}_{i+1}$, is used by the null vector corresponding to two connection configurations in the inverter, i.e. vectors $\mathbf{V}_0$ and $\mathbf{V}_7$ together.

2.4.4.1.2. Sequence list

The applicable sequences for a period are made up of a limited number of phases of variable durations. For a conventional vector PWM, there are only six different sequences (excluding phase duration variations), which correspond to the six sectors identified in Figure 2.14. Generally speaking, a generic sequence associated with sector (i) may take the form:

1) application of vector $\mathbf{V}_0$;

2) application of vector $\mathbf{V}_i$ for odd i and $\mathbf{V}_{i+1}$ if i is even;

3) application of vector $\mathbf{V}_i$ for even i and $\mathbf{V}_{i+1}$ if i is odd;

4) application of vector $\mathbf{V}_7$;

5) application of vector $\mathbf{V}_i$ for even i and $\mathbf{V}_{i+1}$ if i is odd;

6) application of vector $\mathbf{V}_i$ for odd i and $\mathbf{V}_{i+1}$ if i is even;

7) application of vector $\mathbf{V}_0$.

A summary of the six sequences is shown in Figure 2.15.

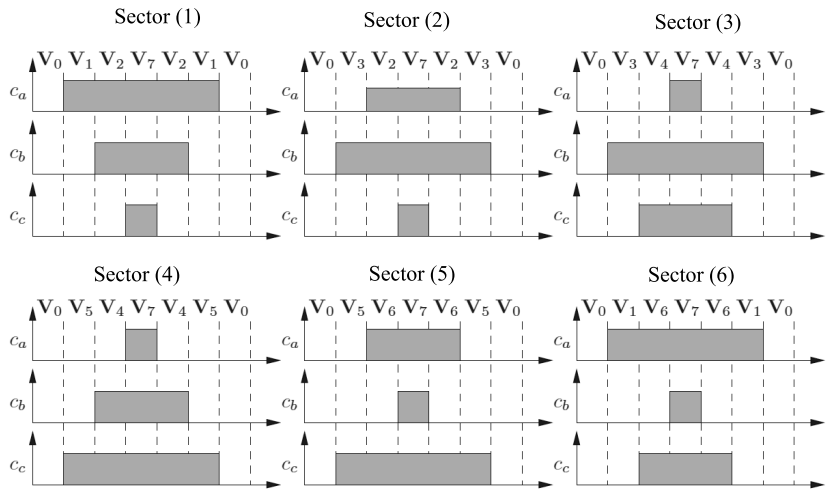


Figure 2.15. *Profiles of control sequences for each sector*

2.4.4.1.3. Limitations

The points in the plane (v_α, v_β) which are accessible to the inverter as average values are included in the hexagon shown in Figure 2.14. $\lambda_i + \lambda_{i+1} = 1$ in the segments connecting the extremities of vectors $\mathbf{V}_1$, $\mathbf{V}_2$, ..., $\mathbf{V}_6$. Leaving the hexagon results in a sequence which exceeds the duration T_d (outlying result).

2.4.4.1.4. Control values

The application durations of vectors $\mathbf{V}_k$ cannot be used directly to control the inverter. It is more practical to consider the durations T_a, T_b and T_c, during which the switching functions c_a, c_b and c_c are equal to 1 for a switching period.

Let $\mathbf{C}[\underline{V}_k]$ be the function linking vector $\mathbf{V}_k$ to the corresponding vector (C). Vector $(T) = (T_a, T_b, T_c)^t$ may then be written in the form:

$$(T) = \sum_{k=0}^{k=7} \lambda_k . T_d . \mathbf{C}[\mathbf{V}_k] \qquad [2.56]$$

where λ_0 and λ_7 are the application durations of vectors $\mathbf{V}_0$ and $\mathbf{V}_7$ (present in all sequences) with $\lambda_0 = \lambda_7 = \frac{1-\lambda_i-\lambda_{i+1}}{2}$ for a sequence in sector (i).

2.4.4.1.5. Digital implementation

The processes involved in vector PWM, as described, are typically digital. This digital aspect goes hand in hand with a discretization of possible states in the plane (v_α, v_β), contrary to what we initially wished to obtain (i.e. continuous regulation of these voltages). Let us now consider a concrete example to see whether this phenomenon will have an effect on the behavior of the "static converter -machine" assembly.

To do this, we will fix a switching period quantification step, equal to $\frac{T_d}{510}$. This enables us to calibrate the duration of the motifs presented in Figure 2.15. These motifs are symmetrical in relation to $\frac{T_d}{2}$, and so the calibration value is limited to a half-period (255 subdivisions of period T_d). We can then code the duration of phase $c_i = 1$" (Bridge i) using $N_b = 8$ bits:

– $00000000_B \Rightarrow c_i = 0$ for the whole of the period T_d;

– $11111111_B \Rightarrow c_i = 1$ for the whole of the period T_d.

From this, we can use the size of the code to deduce the number of available sequences N_s:

$$N_s = \left(2^{N_b}\right)^3 \qquad [2.57]$$

In our example, we have $N_s = 2^{24} = 16.777 \times 10^6$; for $N_b = 4$, we obtain $N_s = 4\,096$. This result is only indicative, in that the number of sequences N_s should not be assimilated to the number N_p of points accessible in the plane (v_α, v_β). In fact, N_p may be expressed as a function of N_b:

$$N_p = \left(2^{N_b+1} - 1\right)^2 - 2^{2N_b} + 2^{N_b} \qquad [2.58]$$

Thus, for $N_b = 4$, we have a number of points $N_p = 721$, as shown in Figure 2.16.

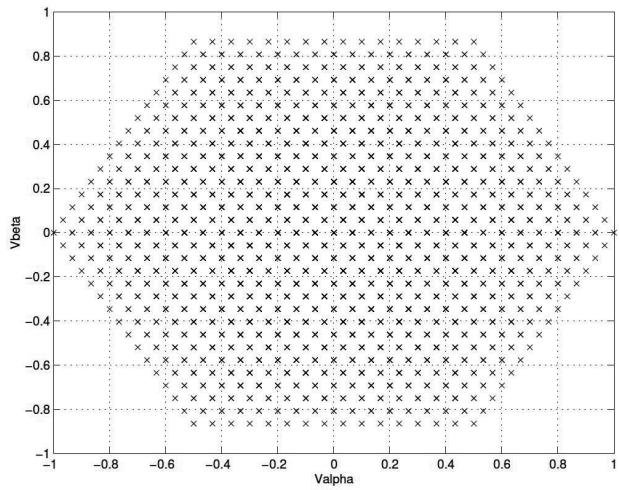


Figure 2.16. *Constellation of points accessible as an average value ($N_b = 4$)*

We will not demonstrate relationship [2.58]. However, it is easy to show that $N_p < N_s$. To do this, let us take the sequences for which the motifs of c_a, c_b and c_c are identical. We have 256 different sequences of this type; these sequences

only include the two vectors $\mathbf{V}_0$ and $\mathbf{V}_7$ together, equal to the null vector. This is an example of losses due to the overlapping phenomenon: these multiple codes all produce the same vector.

The curve in Figure 2.17 gives the number of points N_p as a function of the number of bits N_b in the code. The line is produced using a logarithmic scale on the X axis. Note that the point distribution is similar to that in Figure 2.16 whatever the number of bytes N_b.

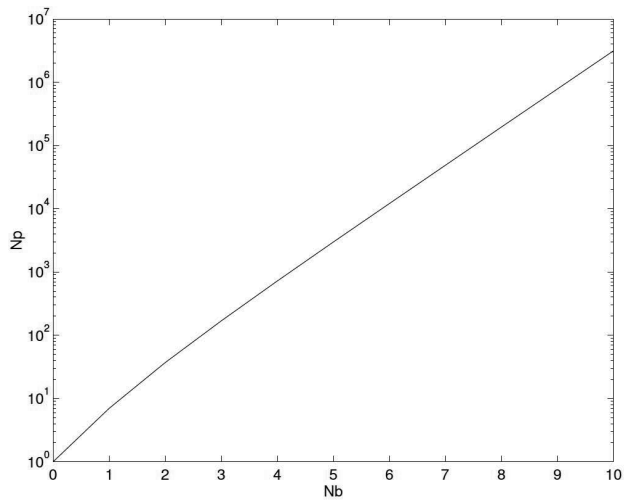


Figure 2.17. *Number N_p of points as a function of the size N_b of the associated code*

However, the results show that the impact of discretization is low, and that the size of the code is not critical. Thus, coding using 8 bits (or fewer) is more than sufficient for the digital modulation operation to be transparent for other system components (controller and machine).

2.4.5. *Geometric analysis of the inverter and PWMs*

One interesting approach to modeling three-phase inverters consists of representing the state of the inverter by

an operating point in a three-dimensional (3D) space. As we have seen, the state of the inverter depends solely on the switching functions driving the three half-bridges of the converter. We can assimilate the switching functions to coordinates in the space $(\mathbf{e}_x, \mathbf{e}_y, \mathbf{e}_z)$. Given that these switching functions c_x with $x \in \{a, b, c\}$ can only take values of 0 or 1, we obtain a discrete operating domain with eight possible positions, marking the vertices of a cube with sides of 1 unit in length. This (dimensionless) cube can also be used to represent the voltages v_{xM}; in this case, the length of the sides of the cube (in volts) is equal to U_0. The average model of the inverter may also be represented geometrically, noting that the average values of the switching functions c_x at the level of the switching period T_d are the associated duty ratios α_x in pulse width modulation. The average state of the converter therefore no longer belongs to a discrete domain, but to a continuous domain, which is the whole of the volume contained in the cube with sides of 1 unit in length (see Figure 2.18).

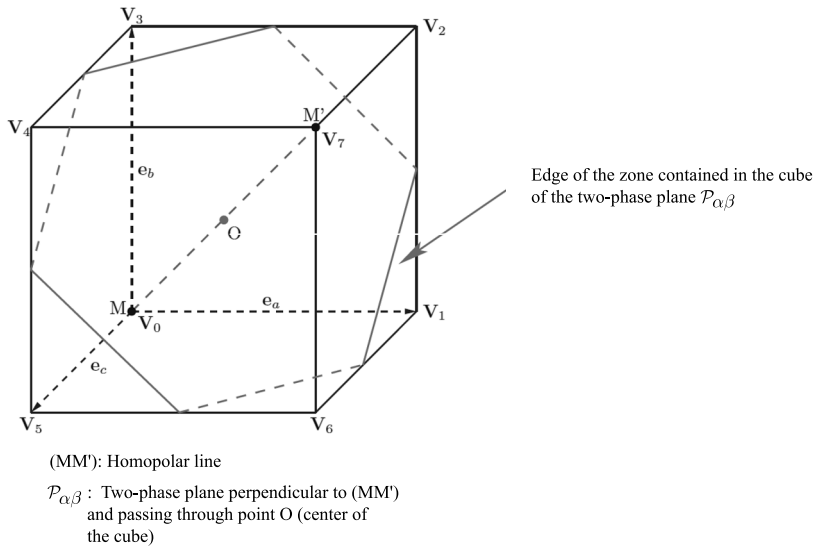


Figure 2.18. *Operating space of the three-phase inverter. For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

On this cube, we have identified points corresponding to the different $\mathbf{V}_k$ vectors ($0 \leq k \leq 7$), and we see that the two vectors $\mathbf{V}_0$ and $\mathbf{V}_7$, which correspond to the coordinates $(0,0,0)$ and $(1,1,1)$, define a straight line with the orientation vector C_{31}: this is the "zero sequence line" defined by the Clarke transform. The vectors forming C_{32} are orthogonal toC_{31} (since $C_{31}^t C_{32} = (0\,0)$), so the two-phase plane (α, β) is perpendicular to this line.

For positioning purposes, we need to define a point of passage; to do this, we simply note that the average value of the voltages produced in sinusoidal PWM (PWM with no zero sequence components in the control signals, except the phase shift of 0.5 for the duty ratios) is equal to $U_0/2$. By applying Millman's theorem to the neutral point of the load, we see that $v_{NM} = U_0/2$ (for a balanced load). Consequently, the identified point of passage of the two-phase plane is simply the center of the cube. Once the normal direction and the point of passage have been established (in the center of the diagonal of the cube defining the zero sequence line), we can easily identify the zone of the plane included in the cube: this is one of the hexagons shown in Figure 2.19.

Figure 2.19 shows the cube from Figure 2.18, this time seen in the axis $\overrightarrow{M'M}$. Points M and M' are thus combined, and the profile of the cube appears having a shape of an hexagon formed by six sides, with vertices corresponding to the "active" vectors from $\mathbf{V}_1$ to $\mathbf{V}_6$ (corresponding to the hexagon defined in Figure 2.18. We also see that the hexagon delimits the part of the two-phase plane $\mathcal{P}_{\alpha\beta}$ contained in the cube: this limit of the two-phase plane corresponds to a maximum norm of vector $\mathbf{v}_{2N}^{ref}$ in the case of sinusoidal PWM. With this strategy, the inverter control scheme does not include a zero sequence component (with the exception of a constant equal to 0.5): the trajectory of the inverter state is consequently flat and contained within this hexagon.

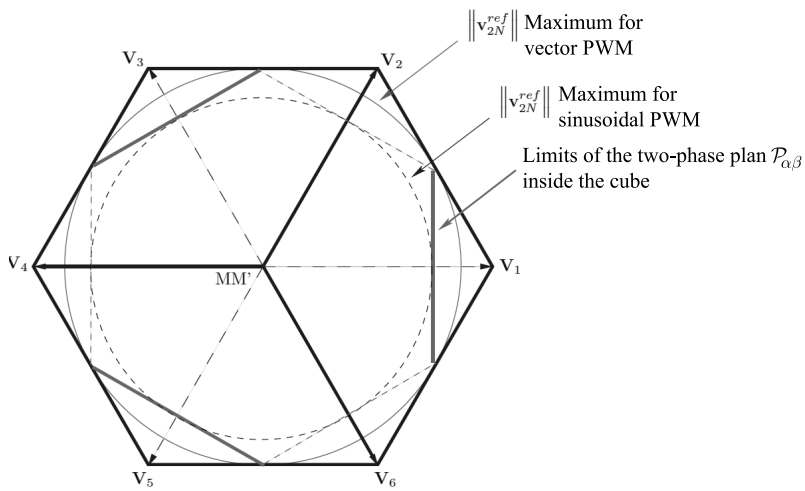


Figure 2.19. *Operating space of the three-phase inverter (view using the hompolar axis). For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

This strategy is not optimal. The inclusion of a zero sequence component in the control scheme is perfectly acceptable, as it does not affect the load. The state of the inverter is therefore allowed to move throughout the whole cube; we see from Figure 2.19 that in this way, the norm of vector $\mathbf{v}_{2N}^{ref}$ is able to reach higher values (without saturation).

2.4.6. *Summary of modulation techniques*

A comparison of modulation strategies for single-phase inverters is given in Table 2.2. PWM strategies (sinusoidal and vector) allow us to obtain a spectrum in which the range of low frequencies only contains the useful term, while unwanted harmonics are restricted to high frequencies. However, this advantage over full-wave modulation is obtained at the expense of the amplitude of the fundamental component of the voltages applied to the load.

2.5. Impact of the inverter on the DC bus

The primary function of an inverter is to supply a voltage to a load, but it also has an impact on its power supply by absorbing a hashed current. The spectral content of this current depends on the type of inverter used (single- or three-phase), but also on the modulation strategy used in controlling it.

2.5.1. *Single-phase inverters*

In the case of the single-phase inverter presented in Figure 2.1 (H bridge), the current i_{dc} absorbed by the DC bus may take three distinct values, which are (taking i_{load} as the current in the load):

$$i_{load} = \begin{cases} i_{load} \text{ if } K_1 = K_4 = \overline{K_2} = \overline{K_3} = 1 \\ 0 \text{ if } K_1 = K_2 = \overline{K_3} = \overline{K_4} = 1 \text{ or } K_1 = K_2 = \overline{K_3} = \overline{K_4} = 0 \\ -i_{load} \text{ if } K_1 = K_4 = \overline{K_2} = \overline{K_3} = 0 \end{cases} \quad [2.59]$$

Therefore, we have HF chopping of the current taken from the DC bus, but it is important to note that the inverter absorbs not only a non-null average current, but also a fluctuating low-frequency component. We must simply note that if the voltage v_{load}^{BF} takes the form:

$$v_{load}^{BF}(t) = V_{\max}.\cos(\omega t) \quad [2.60]$$

and the load consumes a current:

$$i_{load}(t) = I_{\max}.\cos(\omega t - \varphi) \quad [2.61]$$

then the instantaneous power p_{load} is written as:

$$p_{load}(t) = V_{\max}.I_{\max}.\cos(\omega t).\cos(\omega t - \varphi)$$
$$= \frac{V_{\max}.I_{\max}}{2}(\cos(2\omega t - \varphi) + \cos\varphi) \quad [2.62]$$

Strategies	Ampl. norm. of plane voltages V_{max}/U_0	Advantages	Disadvantages
Sinus. PWM (SPWM)	$\frac{1}{2} = 0.5$	Simplicity of creation (analog or digital circuit), high spectrum quality	Limited voltage amplitude, switching losses
Vector PWM (SV-PWM)	$\frac{1}{\sqrt{3}} \approx 0.577$	Maximum voltage amplitude for linear PWM, high spectrum quality	Complexity (digital circuit quasi-compulsory), switching losses
Full wave modulation	$\frac{2}{\pi} \approx 0.637$	Maximum fundamental amplitude, reduced switching losses, simplicity	Poor spectrum quality

Table 2.2. *Comparison of modulation techniques for a three-phase inverter*

If we consider that the inverter has a unitary yield, then the instantaneous power $p_{dc}(t)$ on the continuous bus is equal to $p_{load}(t)$. Presuming that the bus voltage is strictly constant and equal to E, we may write:

$$p_{dc}(t) = E.i_{dc}(t) \quad [2.63]$$

Evidently, this equation conceals the HF phenomena involved in chopping, and it is better to use the current $i_{dc}^{BF}(t)$, expressed as follows:

$$i_{dc}^{BF}(t) = \frac{V_{\max}.I_{\max}}{2E}\left(\cos\left(2\omega t - \varphi\right) + \cos\varphi\right) \qquad [2.64]$$

We therefore have a component at two times the fundamental frequency, in addition to the continuous component. Filtering must therefore take account of this LF component, as it has the highest impact on the voltage wave at the terminals of the decoupling capacitor, which should be placed directly at the entry to the inverter. In these conditions, HF switching has comparatively little effect.

2.5.2. *Three-phase inverters*

In the case of a three-phase inverter, we can easily show the absence of fluctuating components. Consequently, the LF current only includes a continuous component. The decoupling capacitor is dimension-based uniquely on the high frequency (HF) current associated with switching. The vector model of the inverter is particularly useful in this case with regard to the continuous bus. We begin by noting that:

$$\mathbf{v}_{2N} = \frac{2U_0}{3}.C_{32}^{t}.\mathbf{c}_3 \qquad [2.65]$$

Using Clarke's formalism, if $\mathbf{i}_2$ is the two-phase current injected into the load, then the instantaneous power in the load is written as:

$$p_{load} = \frac{3}{2}\mathbf{v}_{2N}^{t}.\mathbf{i}_2 \qquad [2.66]$$

The instantaneous input power is identical, and is written as (for a DC bus voltage U_0):

$$p_{dc} = U_0.i_{dc} \qquad [2.67]$$

hence:

$$i_{dc} = \left(C_{32}^{t}.\mathbf{c}_3\right)^{t}.\mathbf{i}_2 \qquad [2.68]$$

We see that the DC bus current is a scalar product between the vector $\mathbf{i}_2$ and a normalized version of the voltage vector $\mathbf{v}_{2N}$, as we may note that:

$$C_{32}^{t}.\mathbf{c}_3 = \frac{3}{2U_0}\mathbf{v}_{2N} \qquad [2.69]$$

Geometrically, the instantaneous current i_{dc} is obtained by orthogonal projection of the two-phase current vector in the load onto a line, for which the orientation vector is the applied instantaneous voltage vector. We should remember that this model does not make use of averaging across the switching period: it is not an LF model, but an instantaneous representation, valid for all instants.

Figure 2.20 shows an example of the projection of a "current" vector onto two active vectors, leading us to calculate the instantaneous absorbed current as input for the DC bus in both cases.

Note that classic PWM strategies ("two adjacent vectors"[4]) such as sinusoidal and vector PWM give us the same result for the effective value of the fluctuating component of the current i_{dc}. Generally, this current may be written as:

$$i_{dc} = I_{dc} + \delta i_{dc} \qquad [2.70]$$

where I_{dc} is the average value of i_{dc} and δi_{dc}, the alternating component. This component is involved in the dimensioning of decoupling capacitors, as if the inverter input filter is correctly dimensioned, the current from the power supply will

4 These strategies use two consecutive active vectors for a switching period, with the addition of one or two null vectors.

be limited to the continuous component, and the whole component δi_{dc} will circulate through the capacitor(s). It is thus important to characterize this component in terms of effective value, as this is the key point used when selecting a capacitor, based on manufacturer specifications[5].

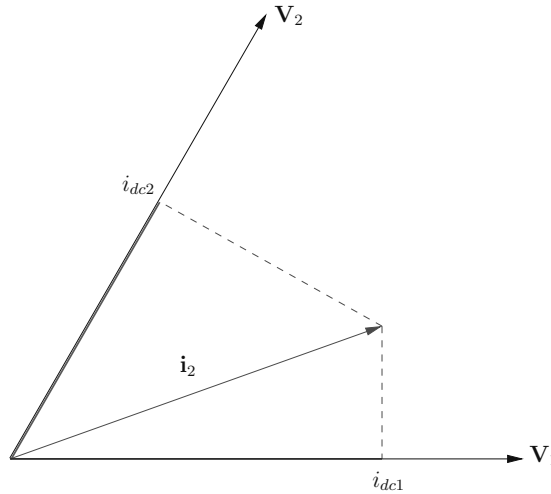


Figure 2.20. *Partial representation of plane* (α, β) *and projections of the "current" vector. For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

Let I_c be the current in the capacitors, and let us suppose that $I_c = \delta i_{dc}$. The RMS of the current is expressed as follows:

$$RMS\left(I_c\right) = I_{\max} \cdot \sqrt{\frac{\sqrt{3}m}{4\pi} + \left(\frac{\sqrt{3}m}{\pi} - \frac{9m^2}{16}\right)\cos^2\varphi} \quad [2.71]$$

This result corresponds to the most widespread PWM strategies, but other strategies (double carrier strategies) exist

5 Spectral distribution is also important, but this is reduced if the capacitor technology is selected with consideration for the switching frequency.

which aim to minimize this criterion [HOB 05, NGU 11a]. These approaches notably work by reducing the application time of the null vectors. These times may even be removed completely when seeking to obtain a high amplitude voltage vector. The current reduction in decoupling capacitors can reach 40%, allowing us to either:

– reduce capacitor volumes (for a given stress);

– increase capacitor lifetime by reducing stress (for a given volume).

2.6. Classification of PWM strategies: overview

The PWM strategies seen above are only some of the techniques which may be applied to electronic power converters. They may be considered as "open loop" controls, as we calculate the control inputs applied to the switches based solely on the reference voltage for the load. This category of control strategies contrasts with the closed loop approach, where a measure (generally of voltage or current) is compared to a reference value, and this comparison (i.e. an error signal) is used to establish the required switch control inputs via a closed loop controller (such as a PI controller, widely used in industrial applications). More recent research activities have led to the creation of another category of mixed, hybrid or semi-open strategies, founded on the concept of carrier-based PWM; in this approach, reference values are established in an open loop, but the choice of a zero sequence component and/or carrier is made based on measurements (generally of current). A classification of the PWM families found in the relevant literature is given in Figure 2.21. This is an updated version of a tree diagram found in Christophe Lesbroussards doctoral thesis, presented at the UTC in 1997 [LES 97].

We have only considered examples from the open-loop group of control strategies in this chapter, specifically:

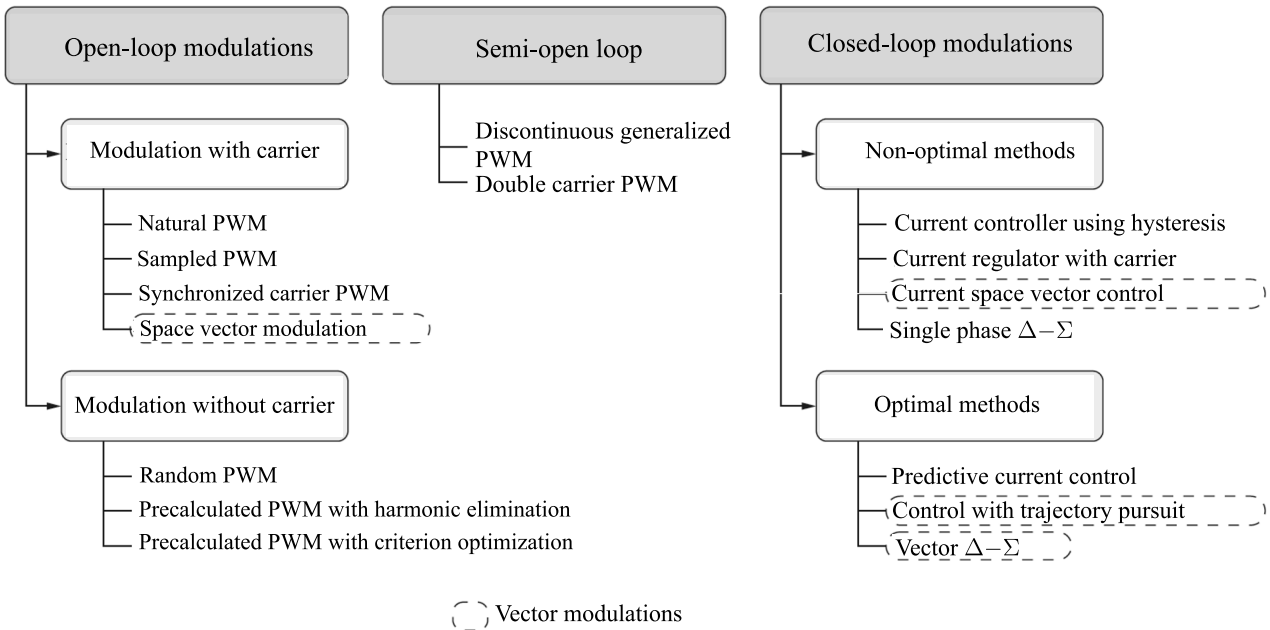


Figure 2.21. *Classification of PWM strategies for a three-phase inverter*

– intersective PWM (which covers natural or uniform sampling);

– precalculated PWM (with harmonic elimination and criteria optimization)[6];

– space vector PWM (also known as space vector modulation, or barycentric PWM).

In reality, intersective PWM strategies, as presented in section 2.2.2, may be used in both analog and digital environments. In an analog context, we use circuits (for example using operational amplifiers) to create a triangular or zigzag carrier, which is compared to an analog signal. This signal itself is produced in a similar way, although it is possible, particularly in the context of three-phase inverters, to use semi-analog methods. These approaches use digital-analog converter circuits, associated with "memories" containing digital tables of waveforms (e.g. sinusoidal waveforms).

Clearly, this type of solution is now obsolete, and purely digital implementations are now used in micro-controllers or programmable logic circuits (CPLD or FPGA). This requires certain adaptations to the strategy; in a microcontroller, even if it includes a timer allowing us to create a digital triangular or zigzag carrier (with a counter, the operating timescales of the timer and the control algorithm are very different. This means that the modulation signal is modified only once or twice per switching period. In this case, we consider that this signal is sampled (hence "sampled PWM") with control loops (typically used to control the torque, speed and/or position of an electrical machine).

We have shown that space vector PWM allows us to optimize the use of the voltage available as input into the

6 This subcategory was described briefly in section 2.2.3.

inverter, with a maximum output voltage which is 15% higher than that obtained using intersective PWM with a sinusoidal modulation signal, while still using a linear operating mode (i.e. without over-modulation, avoiding saturation of the signal). To achieve this, the control strategy takes account of the converter as a whole, rather than controlling individual half-bridges independently, as we might expect given the modular construction of a three-bridge three-phase inverter. However, note that the vector-based vision of inverter control is not really better than that based on intersective PWM, as an equivalent result may be obtained by adding a zero sequence component of the form:

$$v_o(t) = \frac{1}{2}\min\left(|v_a|, |v_b|, |v_c|\right) \qquad [2.72]$$

to the sinusoidal modulation signals v_a, v_b and v_c used in classic intersective PWM, following the diagram shown in Figure 2.22.

Furthermore, although it is possible to implement a purely vector-based intersective PWM strategy using a microcontroller [MIC 05], an equivalent intersective PWM implementation is often preferred [MON 97] as this approach is less costly in calculation terms. Vector-based and intersective approaches may therefore be considered complementary for understanding the operation of an inverter for a given control, from both load and source perspectives, and for synthesizing control laws.

Note that classical space vector modulation requires both null vectors to be used for identical time periods per switching periods. This arbitrary choice implies that each half-bridge is switched twice per period.

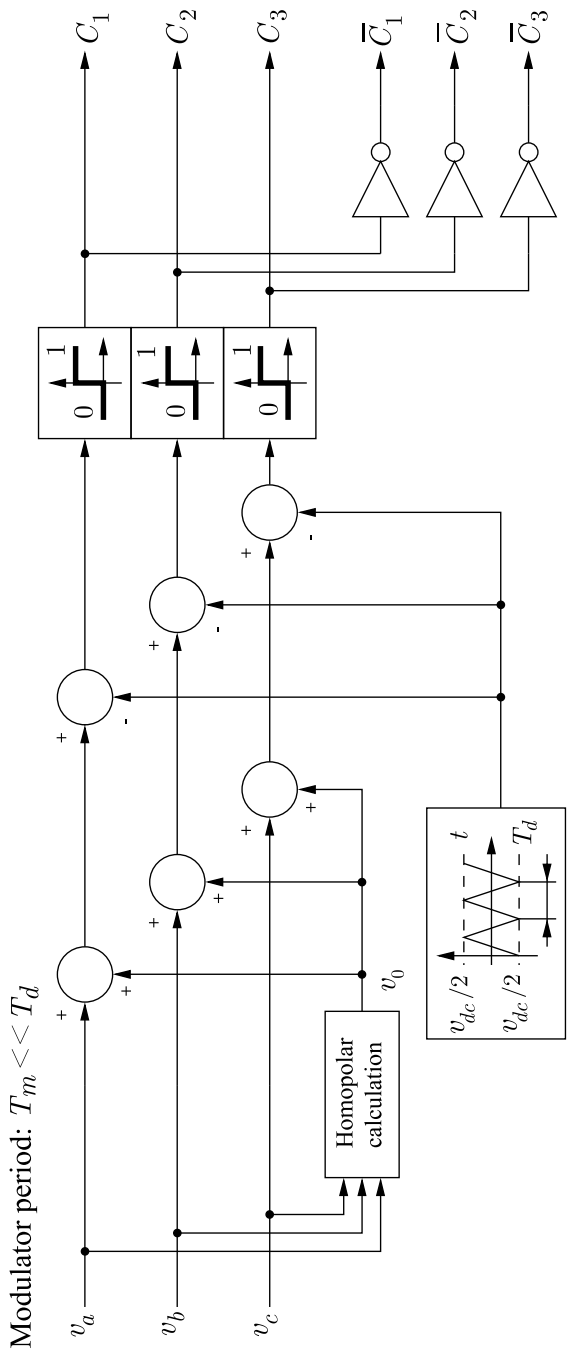


Figure 2.22. *Intersective PWM with injection of a zero sequence component*

It would, however, be perfectly possible to use only one of the two null vectors without affecting the voltage applied to the load: this is the principle of discontinuous PWM (DPWM). In this case, we might expect a reduction in switching losses, as one half-bridge is maintained in a constant state throughout each switching period (the half-bridge with the highest or lowest modulation signal). Different variants of DPWM strategies exist, but a generalized approach (GDPWM) systematically minimizes switching losses, the main goal for this type of modulation. A solution given in [NGU 11b] consists of measuring the current circulating in the half-bridge with the highest modulation signal, alongside the current in the half-bridge with the lowest modulation signal. Either half-bridge may be switched on; it is best to use the half-bridge carrying the highest current in absolute terms, as switching losses are proportional to the switched current. Switching on the half-bridge with the highest current therefore results in minimum losses. These losses are also lower for DPWM than for classic PWM, which systematically switches all three half-bridges in each switching period. This is neither a truly open-loop control strategy, as the control signals depend on a measurement (in this case, that of the current injected into each of the two half-bridges); nor is it a truly closed-loop approach, as currents are never directly regulated.

A variety of "open loop" type strategies exist, acting on control signals based on measurements. Another group of strategies of this type, studied in the LEC at the UTC [HOB 05, NGU 11a], concerns the reduction of the effective current in decoupling capacitors. These control schemes use "classic" intersective PWM, but use two (opposite) carriers for each of the three half-bridges, while the classic approach uses a single carrier. These strategies (a number of variations exist) formed the basis of two theses, which demonstrated that the use of three active vectors, or of two non-consecutive active vectors and a null vector, leads to significant

reductions in the effective value of the AC component of inverter input: consequently, the current circulating in the switching capacitors of the DC bus[7].

Finally, the only constraint which may reasonably be imposed for inverter control is that the two half-bridges should not switch simultaneously (see the diagram of possible switches in Figure 2.23). This is not due to the potential for damage to the inverter (except in relation to increased EMC disturbances), but rather to the fact that we cannot guarantee that two half-bridges will switch at exactly the same moment; this raises the possibility of more or less erratic intermediate states[8].

For closed-loop control techniques, values are systematically controlled in order to follow a reference value. To do this, the value in question is measured, then compared to a reference value. The error between the two values is used by the controller (e.g. a PI controller). Once again, a number of variations are possible, as shown in the table in Figure 2.21. We will consider these approaches in the following section.

2.7. Closed-loop control

2.7.1. *Definitions and classification*

Generally speaking, closed-loop converter control aims to regulate (control) a voltage or voltages, or more generally the output current(s), in an attempt to achieve a reference value, independently of disturbances such as voltage dropoffs in

7 This current (more specifically its effective value) is a key parameter in dimensioning capacitors, as we will see in our case study of a variable speed drive, presented in Chapter 6.

8 These states may or may not be problematic. In the latter case, no restrictions are needed, and a wide variety of PWM strategies may be envisaged.

switches, deadtime introduced by IGBT/MOSFET drivers or fluctuations in the inverter input voltage. The only constraint in attaining this objective is the need to physically possess the dynamic performances needed to follow the reference value, along with sufficient bandwidth in the regulation (control) loop to process the reference values and disturbances.

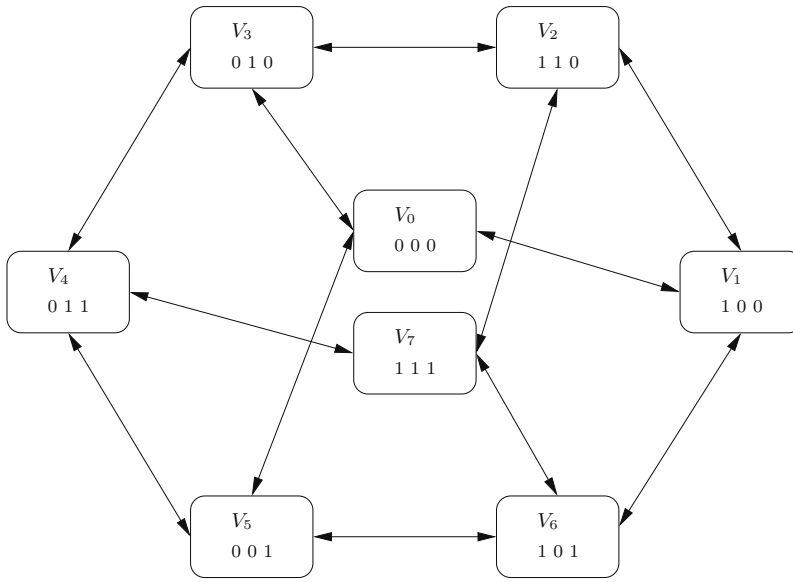


Figure 2.23. *Diagram of "authorized" switches*

In Figure 2.21, the closed-loop family of control strategies is split into two categories, labeled "optimal" and "sub-optimal". It is important to establish a clear definition of the notion of optimality in this context. Strategies considered to be optimal are those which combine the vector aspect of control (and therefore use a global approach to the control of the three half-bridges) with direct control of switches, without the use of carrier-based PWM, which hides the instantaneous behavior of the converter, instead providing an "averaged" vision.

2.7.2. *Non-optimal controls*

2.7.2.1. *Hysteresis control*

The first type of non-optimal control cited in our list is hysteresis control. This is a form of direct switch control (i.e. without a carrier), but it involves controlling each current (at each half-bridge output) independently. The structure of the controller is shown in Figure 2.24.

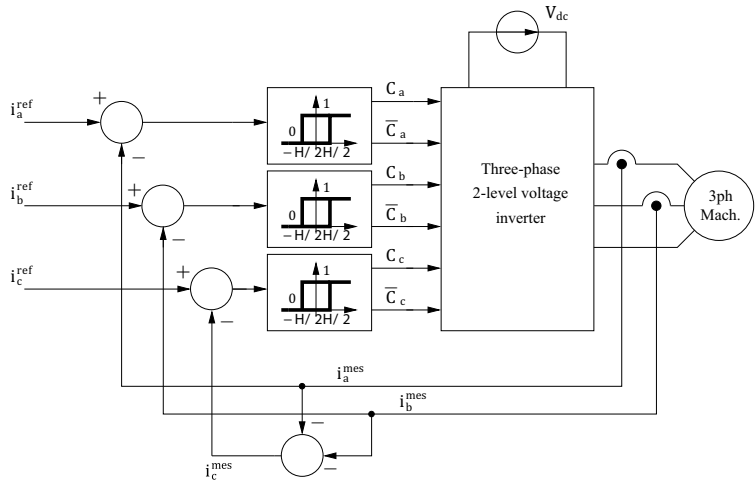


Figure 2.24. *Three-phase hysteresis control*

The hysteresis controller behaves in an intuitive manner, applying a switching function equal to one to increase the current and a value of 0 to reduce the current. This control scheme is particularly robust in relation to uncertainties regarding load parameters, and, from an “automatic control” viewpoint, belongs to the “sliding control mode” category. This control method is highly dynamic, but the current ripple is linked to the width of the hysteresis and the switching frequency increases as the hysteresis window narrows. Current ripples may be reduced, but at a cost: switching losses in the switches increase in proportion to the reduction. Moreover, in qualitative terms, the frequency will increase or decrease according to the width of the hysteresis, but we

cannot precisely control this frequency, which fluctuates as a function of variations in the reference values and of variations in load parameters. It is therefore difficult to precisely control the spectrum of switched quantities (output voltages, input current); this may have undesirable consequences in terms of EMC, or in terms of the vibration and noise associated with the use of this type of power supply in a machine.

REMARK 2.7.– The controlled quantities (the three currents) are linked by a zero sum, so the three currents cannot be controlled independently in three hysteresis windows. In practice, a controller of this type, duplicated three times for the three half-bridges, will not be able to operate strictly with each current i_k with $k \in a, b, c$ such that $i_k^{ref} - i_k^{mes} < H/2$. Figure 2.25 shows a simulation of this control approach in an ideal inverter, connected to an ideal voltage source (input) and with a three-phase RL load as output. The currents are not confined to an interval $[-H/2; +H/2]$ around the reference value ($H = 0.25$A in this case).

2.7.2.2. *Carrier-based current regulation*

One more traditional solution for current regulation consists of using a PWM of the type considered above (such as sinusoidal intersective PWM or vector PWM), for which voltage reference values are established by current control loops in each phase. Generally, PID controllers are used for this operation (PI controllers are also widely used in electrical engineering). However, we should note that, while these controllers offer good performances in regulating values in relation to a constant reference value (no static error), they do not perform as well when following a variable reference value (following error), particularly in the case of sinusoidal variation.

We should remember that the function used to obtain a closed-loop of unity feedback system $T_{CL}(p)$ (see Figure 2.26)

from an open-loop transfer function $T_{OL}(p)$ is expressed as follows:

$$T_{CL}(p) = \frac{T_{OL}(p)}{1 + T_{OL}(p)} \qquad [2.73]$$

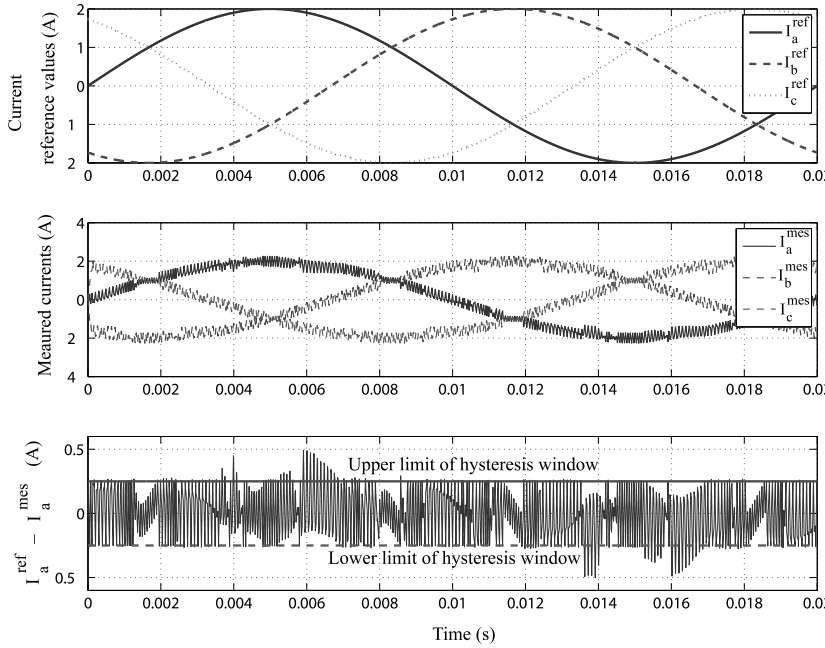


Figure 2.25. *Simulation of three-phase hysteresis control for $H = 0.5A$ and $I_{\max}^{ref} = 2A$ for a series load $R = 1\,\Omega$, $L = 1\,mH$. For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

In order to follow the reference value exactly, the closed-loop transfer function must be equal to 1, and thus the function $T_{OL}(p)$ must tend toward infinity for the frequency of the input signal (while guaranteeing stable operations). This result is obtained using a PI controller for constant input, but is not achieved when using a sinusoidal signal. In this case, the solution is to use a filter which resonates at the frequency of the reference signal.

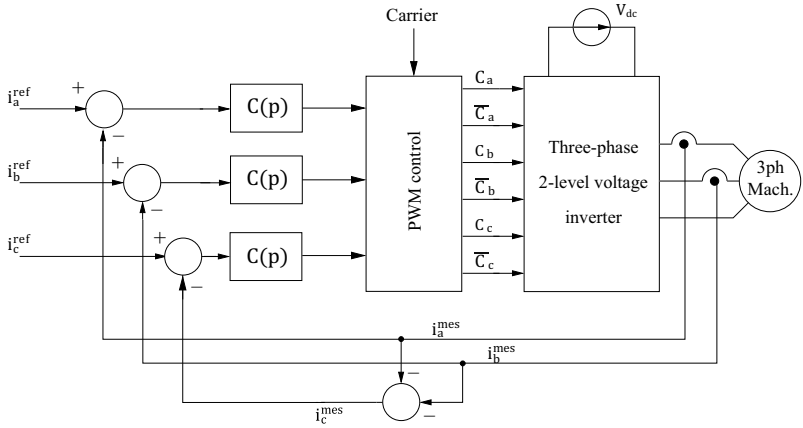


Figure 2.26. *Generic structure for current control using intersective PWM*

In fact, satisfactory results can be obtained using a PI controller on the condition that the reference signal is located within the bandwidth of the closed loop. Figure 2.27 shows simulation results obtained using a PI transfer function:

$$C(p) = K_p \frac{1 + T_i p}{T_i p} \qquad [2.74]$$

where the chosen value of T_i is equal to the time constant of the load ($T_i = \tau = L/R$). This is known as pole compensation control. We then choose to take $K_p = 1$. In these conditions, we obtain an open-loop transfer function of the form:

$$T_{OL}(p) = \frac{G_{inv}}{\tau p} \qquad [2.75]$$

where G_{inv} is the inverter gain connecting the amplitude of reference values at the input of the PWM controller and the voltages supplied as output. In our case, the input signals are normalized between -1 and 1, while the output voltages have a maximum amplitude of $V_{dc}/2$. The inverter gain is therefore

equal to $V_{dc}/2$ (25 V in our simulation). The RL load is parameterized as follows:

$$\begin{cases} R = 10\,\Omega \\ L = 1\,\text{mH} \end{cases} \quad [2.76]$$

The time constant is therefore equal to $100\,\mu$s. From this, we may deduce a closed-loop transfer function of the form:

$$T_{CL}\,(p) = \frac{\frac{G_{inv}}{\tau p}}{1 + \frac{G_{inv}}{\tau p}} = \frac{1}{1 + \frac{\tau}{G_{inv}} p} \quad [2.77]$$

We thus obtain a time constant of $4\,\mu$s, and the bandwidth of the closed loop is therefore 39.7 kHz. This bandwidth appears sufficient to control currents of up to a few hundred Hertz; this is confirmed by simulation results, as shown in Figure 2.27 for two reference values with an amplitude of 2 A at frequencies of 50 and 200 Hz respectively.

There is only a small lag between the reference and measured values at 200 Hz (although this is hard to measure with switching). We can verify this lag theoretically, as it is equal to:

$$\varphi_{200\text{Hz}} = -\arctan\left(\frac{2\tau\pi \times 200}{G_{inv}}\right) = -0.3° \quad [2.78]$$

This situation is suited to the use of a PI controller, as the time constant of the load is already relatively low. This is not always the case, and in these situations, we need to use a resonating filter instead of the PI controller. The transfer function of this type of controller must include a factor of the form:

$$C_{net}(p) = \frac{1}{1 + (p/\omega_{net})^2} \quad [2.79]$$

This corrector presents an infinite gain at angular frequency ω_{net}, so the closed-loop transfer function is equal to 1 for this precise angular frequency. We can therefore follow a sinusoid at this frequency with no error[9].

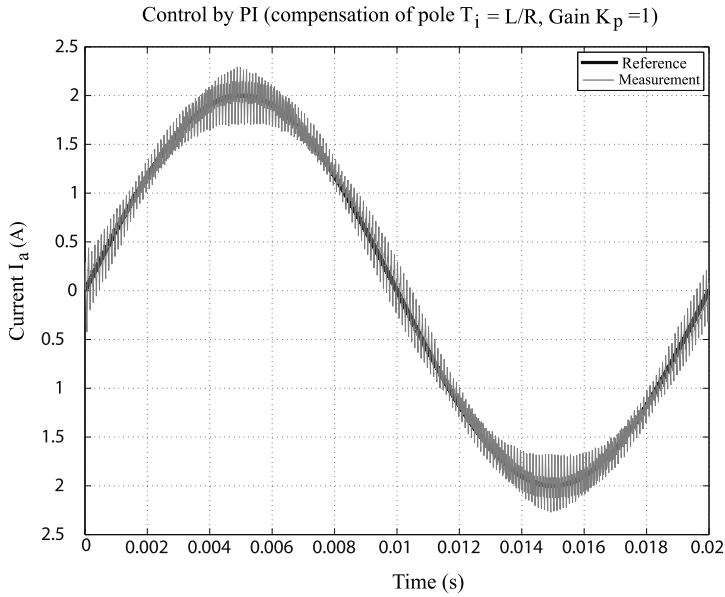


Figure 2.27. *Simulation of three-phase hysteresis control for* $H = 0.5A$ *and* $I_{\max}^{ref} = 2A$ *for a series load* $R = 1\,\Omega$, $L = 1\,mH$

2.7.2.3. *Controlling the current space vector*

A more effective means of controlling currents via a PI corrector, independently of the parameters of the physical system, consists of observing sinusoidal values in a reference frame rotating at the same speed. This is the Park transform (abc-to-dq transformation), which consists of two successive steps:

– transformation from three phases "abc" to two phases "$\alpha\beta$" (Clarke or Concordia transform);

9 Ripples due to switching introduced by PWM will still be present.

– rotation of the fixed two-phase frame of reference $\alpha\beta$ to a rotating two-phase frame, generally noted *dq*.

In these conditions, sinusoidal values are seen as constant values, which can be controlled with no following error by a PI controller. We may easily verify the connection between the abc and *dq* values in permanent sinusoidal mode, taking a balanced, direct three-phase system in vector form:

$$\mathbf{x}_3 = X_{\max}. \begin{pmatrix} \cos\alpha \\ \cos\left(\alpha - 2\pi/3\right) \\ \cos\left(\alpha + 2\pi/3\right) \end{pmatrix} = X_{\max} C_{32}. \begin{pmatrix} \cos\alpha \\ \sin\alpha \end{pmatrix} \quad [2.80]$$

Note that the rotation matrix $P(\alpha)$ is defined as follows:

$$P(\alpha) = \begin{pmatrix} \cos\alpha & -\sin\alpha \\ \sin\alpha & \cos\alpha \end{pmatrix} \quad [2.81]$$

We can therefore note that:

$$\begin{pmatrix} \cos\alpha \\ \sin\alpha \end{pmatrix} = \begin{pmatrix} \cos\alpha & -\sin\alpha \\ \sin\alpha & \cos\alpha \end{pmatrix} . \begin{pmatrix} 1 \\ 0 \end{pmatrix} \quad [2.82]$$

and thus:

$$\mathbf{x}_3 = X_{\max} C_{32}.P\left(\alpha\right). \begin{pmatrix} 1 \\ 0 \end{pmatrix} \quad [2.83]$$

By identification with the Park transform (based on the Clarke transformation[10]):

$$\mathbf{x}_3 \triangleq C_{32}.P\left(\alpha\right).\mathbf{x}_{dq} \quad [2.84]$$

10 Which therefore retains the real amplitude values.

where $\mathbf{x}_{dq}$ is the two-phase Park vector equivalent to $\mathbf{x}_3$. By identification, we have, simply:

$$\mathbf{x}_{dq} = \begin{pmatrix} X_{\max} \\ 0 \end{pmatrix} \qquad [2.85]$$

In the case of operation in permanent sinusoidal mode, we simply have $\alpha = \omega.t + \varphi_0$. The controller imposes its own references, and the reference frame may be chosen arbitrarily with a null phase at the origin instant; in this case, only the angular frequency counts, and this should be equal to the desired value (for example Ω/N_p for a synchronous machine where Ω is the mechanical speed of the machine and N_p, the number of pairs of poles in the machine). Then the controller has the structure presented in Figure 2.28.

2.7.2.4. *Single-phase* Σ–Δ *control*

Unlike the closed-loop control structures presented in the previous section, Σ–Δ control operates on the voltage rather than the current. This control strategy is derived from a technique used in analog to digital converters. The principle behind the strategy lies in the observation of the error occurring between the output voltage of the converter (which necessarily belongs to a discrete, and limited, series of values) and a reference value, which may take an infinite number of values within a given interval. This error, noted Δ, is then integrated to produce a signal, noted Σ. The converter is then controlled in such a way that signal Σ remains within a given interval (as in the case of hysteresis control).

Mathematically speaking, these operations involve evaluating the sliding average of the converter output voltage, and making this average follow a reference. This results in closed-loop control of the voltage supplied to the load. It does not allow us to control the current injected into a machine, but this closed loop is able to control the voltage delivered by an inverter, irrespective of disturbances such as:

– variations in the voltage of the DC bus at the converter entry point;

– deadtimes introduced by gate drivers (which tend to reduce the RMS voltage supplied to the load in comparison with ideal waveforms without deadtime);

– voltage dropoffs resulting from switching.

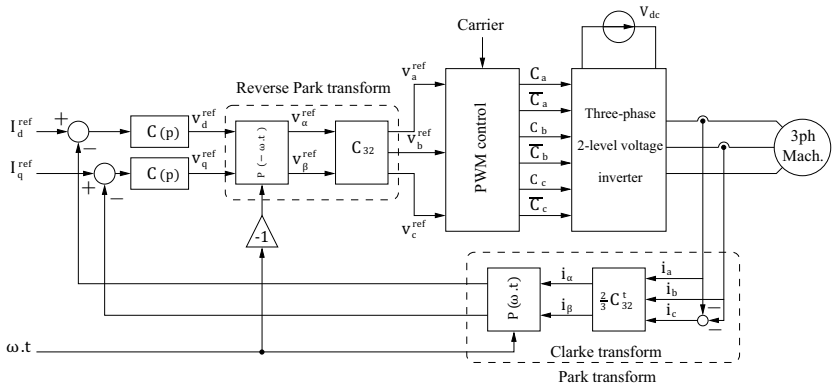


Figure 2.28. *Regulation of currents controlled by an inverter with carrier-based PWM in the plane* dq

One advantage of this control strategy is that it guarantees a high voltage quality (in terms of harmonic distortion) for a low average switching frequency for the switches.

We can therefore apply this single-phase control (also used in single-phase contexts, notably for class D audio amplifier controls) independently to each half-bridge of a three-phase inverter (see Figure 2.29) in the same way as hysteresis or PI controllers are applied to the three currents. However, a vector approach is generally preferred; this strategy will be discussed in section 2.7.3.

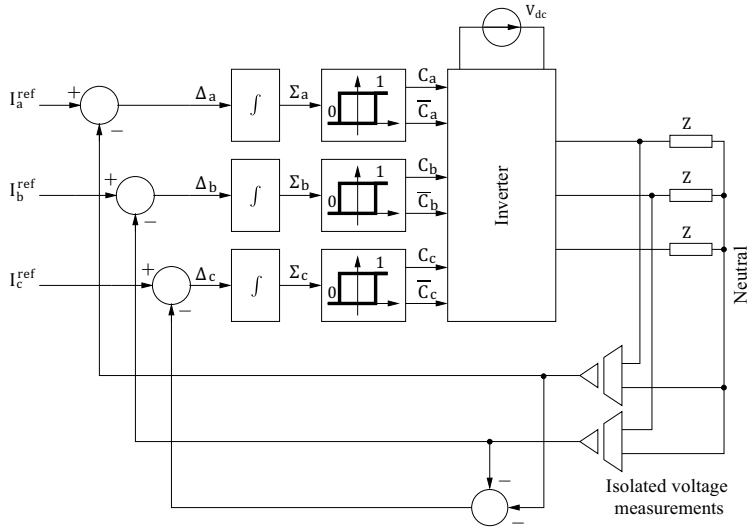


Figure 2.29. *Single-phase Σ–Δ control applied to a three-phase inverter (duplicated three times)*

2.7.3. *Optimal control*

2.7.3.1. *Predictive current control*

Predictive current control was proposed by Holtz and Stadtfeld in [HOL 83] for controlling stator currents in three-phase AC machines. While the approach may be generalized for other contexts, this application constitutes a point of reference; in this section, we will consider the connected machine (or load or source) as a balanced series load R, L, E with a star connection. We will therefore consider that resistances and inductances are identical, and the e.m.fs form a balanced three-phase system. It would be possible to consider non-sinusoidal e.m.fs with a 120° phase shift, but we will consider the e.m.fs to be sinusoidal. The three voltages E_a, E_b and E_c are therefore written as follows:

$$\begin{cases} E_a(t) = E_{\max} \cos \omega t \\ E_b(t) = E_{\max} \cos\left(\omega t - \frac{2\pi}{3}\right) \\ E_c(t) = E_{\max} \cos\left(\omega t + \frac{2\pi}{3}\right) \end{cases} \quad [2.86]$$

As we have seen, a two-level three-phase voltage inverter possesses eight distinct states according to the control input values used (i.e. the three switching functions). From a load perspective, seven different states are available. As the number of control input combinations is finite, we may study the load response to all possible configurations. To do this, we first need to establish an equation model for the load. The best reference frame for this purpose is a two-phase stationary frame $\alpha\beta$ (in this case, we have selected a Clarke transformation). We thus obtain:

$$\mathbf{v}_2 = R.\mathbf{i}_2 + L\frac{d\mathbf{i}_2}{dt} + \mathbf{e}_2 \qquad [2.87]$$

where $\mathbf{v}_2 = (v_\alpha, v_\beta)^t$, $\mathbf{i}_2 = (i_\alpha, i_\beta)^t$ and $\mathbf{e}_2 = (e_\alpha, e_\beta)^t$ and for this vector e.m.f, we can also write, following [2.86]:

$$\mathbf{e}_2 = E_{\max}.\begin{pmatrix}\cos\omega t\\ \sin\omega t\end{pmatrix} \qquad [2.88]$$

On this basis, we know that the voltage vector $\mathbf{v}_2$ can only take seven distinct values, based on the number k of the voltage vector used for the inverter output. Note that k is the value of the control input index, and is an integer between 0 and 7 inclusive.

We note that:

$$\mathbf{v}_2 = 0 \text{ for } k = 0 \text{ or } k = 7 \qquad [2.89]$$

and that:

$$\mathbf{v}_2 = \frac{2U_0}{3}\begin{pmatrix}\cos\left(\frac{(k-1)\pi}{3}\right)\\ \sin\left(\frac{(k-1)\pi}{3}\right)\end{pmatrix} \text{ for } 1 \leq k \leq 6 \qquad [2.90]$$

where U_0 is the voltage of the DC bus at the inverter input point.

Generally speaking, $\mathbf{v}_2[k]$ is therefore the inverter output voltage for a given control input index k. This makes it possible to predict the evolution of currents in the load based on the model [2.87]:

$$\frac{d\mathbf{i}_2}{dt} = \frac{1}{L}\left(\mathbf{v}_2 - R.\mathbf{i}_2 - \mathbf{e}_2\right) \qquad [2.91]$$

We therefore require a model of the load (and thus R and L, which are identifiable, and the vector e.m.f. $\mathbf{e}_2$ which can generally be estimated for a given instant), but we also need to measure the current in order to make a prediction. In theory, a single initial measurement is required, and all predictions can then be based on their predecessors. In practice, however, the context of open-loop operations means that this method will result in erroneous predictions after a given period of time, which varies based on the chosen prediction model[11]. It is therefore better to obtain a new current measurement for each new prediction phase (including all possible values of k). If the time frame of prediction ΔT is sufficiently short, we may approximate the derivative using a rate of increase, and we obtain a prediction for instant t of the current at $t + \Delta T$ for control k:

$$\hat{\mathbf{i}}_2(t + \Delta T, k) = \mathbf{i}_2^{mes}(t) + \frac{\Delta T}{L}\left(\mathbf{v}_2[k] - R.\mathbf{i}_2^{mes}(t) - \mathbf{e}_2(t)\right) \qquad [2.92]$$

These predictions are then compared with a current reference value $\mathbf{i}_2^{ref}$, before making control decisions based on a given criterion. For example, a control signal may be selected with the aim of obtaining the lowest possible switching frequency for a given ripple value in the current vector. This is illustrated in Figure 2.30, which shows the generalized structure of a predictive control, and an

11 This time is very short if we do not take account of imperfections in the inverter and in the close control approach.

illustration of predictions of the evolution of the current vector.

This figure also shows that the selection process consists of choosing the prediction which is most closely directed toward the reference value, and which therefore lengthens the path to the "wall" of the authorized zone around the reference point before the next switching operation.

REMARK 2.8.– Note that this reference point may evolve, and in this case, the circular limit around the reference point also evolves. In this case, the choice made in Figure 2.30 will not necessarily be the best option to reduce the switching frequency. Where possible, it is interesting to plan the trajectory of the reference point, and include this additional information in the decision-making element: this is the notion of control with trajectory pursuit, included in the classification in Figure 2.21.

This control strategy can be generalized to more complex converters (for example an inverter with four half-bridges). In this case, the duplication involved in the converter provides a certain level of fault tolerance (operation in degraded mode). This approach presents major advantages, as predictions are easy to verify *a posteriori*, which enables us to detect abnormal evolutions. In this way, we can both identify and localize faults (i.e. identify the faulty switch), then take account of this information in order to limit future predictions to the controls still available in the faulty converter.

2.7.3.2. *Vector Σ–Δ control*

Vector Σ–Δ control uses the same concept as single-phase Σ–Δ control, which consists of controlling the voltage in a closed loop by integrating the difference between a reference value and a measurement. However, the compared values are now vectors, rather than scalar values. The reference value

and measurement are obtained in a two-phase plane $\alpha\beta$, obtained using a Clarke or Concordia transformation of the real-values.

REMARK 2.9.– Vector integration consists of a scalar integration of each component.

We now need to define the controller. In the case of a scalar Σ–Δ control scheme, as shown in Figure 2.29 (duplicated for the three phases of an inverter), this was a hysteresis comparator. When using vectors, we need to define a type of comparator with a domain of definition suited to the context; this is a 2D domain in the plane $\alpha\beta$. The logical choice is to define limits of the evolution of the error signal Σ in a circle (centered on the origin of the reference frame $\alpha\beta$) to guarantee that the voltage reference value will be followed in the same way as for predictive vector control of currents, shown in Figure 2.30.

Σ–Δ vector control is therefore a closed-loop approach for control of the voltage vector, and does not include a load model; it is therefore only able to compensate for disturbances introduced by fluctuations in the inverter input voltage (noted U_0 in the diagram in Figure 2.30 or modifications in relation to the ideal waveforms introduced by close control of inverters (particularly deadtimes).

REMARK 2.10.– The most significant advantage of Σ–Δ control is that it significantly reduces the required switching frequency, while maintaining a high quality power supply to the load. This strategy is particularly interesting for driving high-powered machines (for example in rail traction or heavy industry), as it requires the use of large components, rated for high voltages and currents, which are generally slow (requiring switching frequencies below 1 kHz).

Several variations on this strategy may be adopted (allowing synchronization with a carrier, or use with

multi-level converters – seen in Chapter 5), but these lie outside the remit of this book. Interested readers may wish to consult [LES 97]. [MON 09] also includes a chapter on Σ–Δ modulation, written by Vilain and Lesbroussard. An English-language version of this work is also available: [MON 11]. This edition is a compilation of two volumes published in French on the subject of PWM and closed-loop control schemes[12] with different current variation techniques.

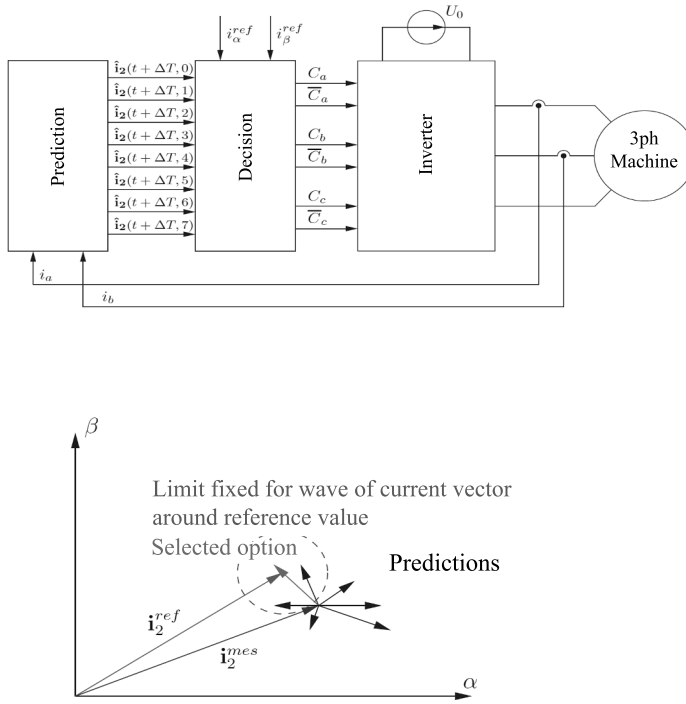


Figure 2.30. *Predictive vector control of currents.*
For a color version of the figure, see www.iste.co.uk/patin/power2.zip

12 In reality, Σ–Δ PWM is also a form of "closed loop" voltage control, unless the voltage output of a half-bridge is assimilated to the corresponding control signal.

3

AC/DC Converters

3.1. Non-controlled rectifiers

3.1.1. *Half-wave rectifiers*

The half-wave rectifier is a converter which carries out half-wave rectification. In a single-phase context, this is a converter including a diode which may be qualified as $\mathrm{P1}$; in a three-phase context, we use $\mathrm{P3}$, and in a generalized case with n phases, $\mathrm{P}n$. A single-phase half-wave rectifier is shown in Figure 3.1. Note that the *alternating current (AC)* side is connected to an ideal voltage source V_r, while the *direct current (DC)* side powers a resistance R. This configuration will also be used for other converters, but we will also study the case of a power supply to a current source I_0 presumed to be constant. Note that in the $P1$ context, it is not possible to power a current source, as this would require permanent conduction through the only diode in the circuit.

The equation model of the only loop in the circuit gives us:

$$V_r = V_{d1} + V_{rec} \qquad [3.1]$$

with:

$$V_{rec} = R.i_{rec} \qquad [3.2]$$

knowing that i_{rec} can only be positive due to the single possible direction of current through diode D_1.

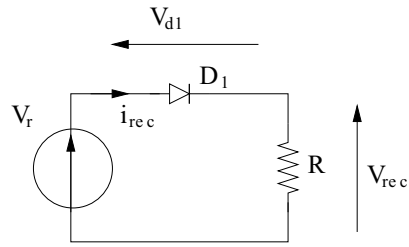


Figure 3.1. *Half-wave single-phase diode rectifier (*P1*)*

In the D_1 OFF state, we know that $i_{rec} = 0$. In this case, we also have $V_{rec} = 0$ and thus $V_r = V_{d1}$. As diode D_1 is switched off for $V_{d1} < 0$, we can write that the switch-off condition for D_1 boils down to:

$$V_r < 0 \qquad [3.3]$$

For state D_1 ON, we know that $V_{d1} = 0$. In this case, we have $V_{rec} = V_r$, and thus $i_{rec} = V_r/R$. As diode D_1 is switched on for $i_{rec} > 0$, we can therefore state that the conduction condition for D_1 is:

$$V_r > 0 \qquad [3.4]$$

For a sinusoidal input voltage V_r of the form:

$$V_r\,(t) = V_{r\max}.\sin\,(2\pi.F.t) \qquad [3.5]$$

this is equivalent to noting, for the interval $0 \leq t \leq T$ (where $T = 1/F$), that:

– D_1 is ON for $0 \leq t \leq T/2$, so we have $V_{rec} = V_r$ and $i_{rec} = V_r/R$;

– D_1 is OFF for $T/2 \leq t \leq T$ with $V_{rec} = 0$ and $i_{rec} = 0$.

An equivalent half-wave rectifier exists for three-phase networks. This is the P3 assembly shown in Figure 3.3. In studying a circuit of this type, we note that the cathodes of diodes D_1, D_2 and D_3 are connected to a common node. Consequently, this group of three diodes (known as a common-cathode cell) can only include one conducting diode (leading to switch off of the two others): this is the diode with the highest potential at the anode. We can therefore write that V_{rec} is equal to the maximum of the three-phase voltages V_{aN}, V_{bN} and V_{cN}:

$$V_{rec} = \max_{x \in \{a,b,c\}} (V_{xN}) \qquad [3.6]$$

Finally, we can write the expression of the average voltages $\langle V_{rec} \rangle$ at the load terminals. Generally, this is written (for a single bridge $\mathrm{P}n$ with $n > 1$ phases) as:

$$\langle V_{rec} \rangle = \frac{nV_{\max}}{\pi} \sin\left(\frac{\pi}{n}\right) \qquad [3.7]$$

where $V_{\max}$ is the amplitude (and not the effective value) of the phase voltages.

This general formula can be applied to the diagram in Figure 3.4. For the P3 bridge, it is, clearly, used as follows:

$$\langle V_{rec} \rangle_{P3} = \frac{3V_{\max}}{\pi} \sin\left(\frac{\pi}{3}\right) = \frac{3V_{\max}\sqrt{3}}{2\pi} \qquad [3.8]$$

This is not applicable to the single-phase context, where we simply use:

$$\langle V_{rec} \rangle_{\mathrm{P1}} = \frac{V_{\max}}{\pi} \qquad [3.9]$$

The waveform of the voltage supplied by the half-wave rectifier is shown in Figure 3.2 for the case of a power supply

of 230 V RMS at 50 Hz. The waveform for the P3 bridge is shown in Figure 3.5.

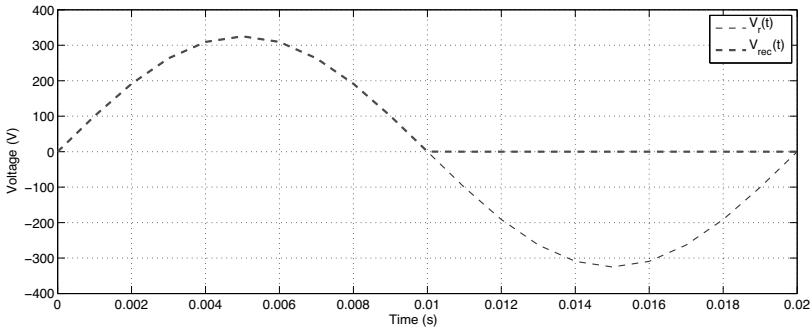


Figure 3.2. *Voltage waveforms for a single-phase half-wave rectifier*

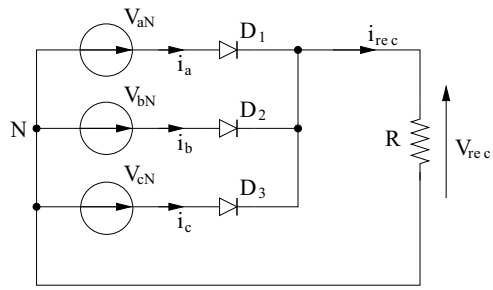


Figure 3.3. *Three-phase half-wave diode rectifier (P3)*

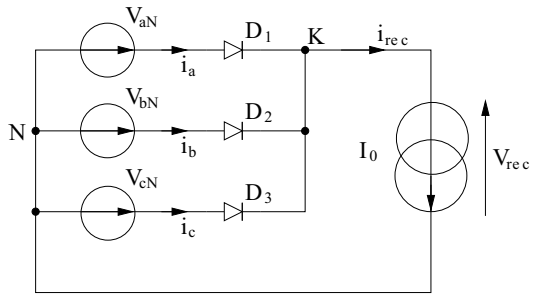


Figure 3.4. *Three-phase half-wave diode rectifier (P3) with current source*

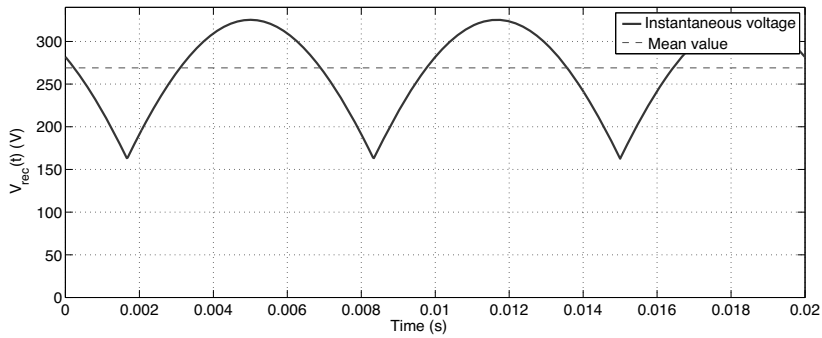


Figure 3.5. *Voltage waveforms for a three-phase, single-alternation rectifier (P3) in a* 230–$400\,V/50\,Hz$ *network*

In terms of currents, we generally consider an ideal case (which may be relatively close to reality) of a power supply with a constant current I_0. In this case, the current absorbed by a phase may be easily expressed as follows:

– either I_0 when the corresponding diode is switched on;

– or 0 when the diode is switched off.

The interest of the corresponding waveforms is limited. However, we may like to consider the power factor (on the source side – denoted as *AC*) of this type of converter, as we can easily calculate the active power, which is the same on the *AC* and *DC* sides as the diodes are presumed to be ideal, i.e. not subject to losses. In the case of the $P1$ bridge, we therefore have:

$$P_{ac}^{\mathrm{P1}} = P_{dc}^{\mathrm{P1}} = \langle V_{rec} \rangle .I_0 = \frac{V_{\max}.I_0}{\pi} \qquad [3.10]$$

For bridge $\mathrm{P3}$, we have:

$$P_{ac}^{\mathrm{P3}} = P_{dc}^{\mathrm{P3}} = \langle V_{rec} \rangle .I_0 = \frac{3V_{\max}.I_0\sqrt{3}}{2\pi} \qquad [3.11]$$

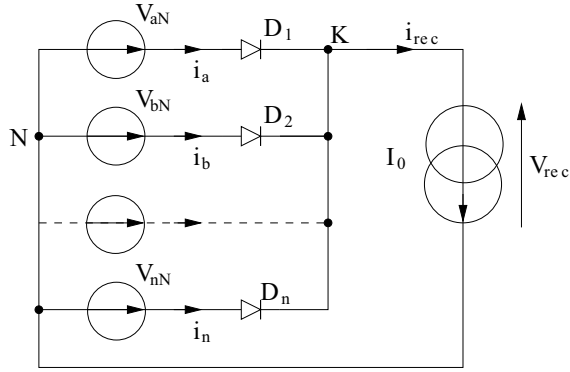


Figure 3.6. *Half-wave n-phase diode rectifier (Pn) with current source*

On the *AC* side, we calculate the apparent power, which is defined in general terms (in non-sinusoidal mode) as follows:

$$S \triangleq \frac{nV_{\max}I_{\mathrm{RMS}}}{\sqrt{2}} \qquad [3.12]$$

where I_{RMS} is the RMS current in a phase. We know (see Appendix 1) that the RMS value of a square periodic signal $x(t)$, with period T and a value of X_0 for a fraction αT of the period and 0 the remaining time, is equal to $X_0\sqrt{\alpha}$. Consequently, we note that:

$$I_{\mathrm{RMS}}^{\mathrm{P1}} = I_0\sqrt{2} \qquad [3.13]$$

and:

$$I_{\mathrm{RMS}}^{\mathrm{P3}} = I_0\sqrt{3} \qquad [3.14]$$

In more general terms, for a bridge $\mathrm{P}n$ with $n > 1$ phases:

$$I_{\mathrm{RMS}}^{\mathrm{P}n} = I_0\sqrt{n} \qquad [3.15]$$

Consequently, we have the following power factor for bridge $\mathrm{P1}$:

$$\lambda_{\mathrm{P1}} = \frac{1}{\pi} \simeq 0,318 \qquad [3.16]$$

and for bridges $\mathrm{P}n$ (with $n > 1$) :

$$\lambda_{\mathrm{P}n} = \frac{\sqrt{2}\sin\left(\frac{\pi}{n}\right)}{\pi\sqrt{n}} \qquad [3.17]$$

In the case of a $\mathrm{P3}$ bridge, this gives us a value of $\frac{1}{\pi\sqrt{2}} \simeq 0,225$. We thus see that the power factor is reduced as the number of phases increases.

REMARK 3.1.– One point which creates significant difficulties for this type of rectifier assembly is the presence of a current component (DC) drawn from the network. This is strictly prohibited in the *Electricité de France* (EDF) (a French electric utility company) network for instance; in the (very frequent) context of installations with a transformer at the top, the circulation of DC currents in the secondary element of a transformer will lead to:

– losses in conductors;

– a displacement of the average magnetic state of the sheets making up the magnetic circuit of the distribution transformer (resulting in a different saturation for positive and negative half-cycles, leading, among other things, to voltage distortions).

3.1.2. *Full-wave bridges*

Full-wave bridges may be studied as an association of two half-wave bridges (one with common cathodes, as above, and the other with common anodes). Note, however, that there is a subtle difference in the naming of double bridges PDn; the single-phase bridge is known as $\mathrm{PD2}$ (which is also known as

a Graetz bridge). The association of the two-phase voltages in this case is clear, as shown in Figure 3.10.

Finally, note that the instantaneous voltage V_{rec} is expressed as:

- V_{aN} when $V_{aN} > 0$;
- $-V_{aN}$ when $V_{aN} < 0$.

In the case of a sinusoidal voltage source V_{aN} (with amplitude $V_{\max}$), we may easily establish the expression of $\langle V_{rec} \rangle$:

$$\langle V_{rec} \rangle = \frac{2V_{\max}}{\pi} \qquad [3.18]$$

Figure 3.7 shows the waveform obtained for a $230\,\mathrm{V}$ RMS sinusoidal voltage at $50\mathrm{H\,z}$.

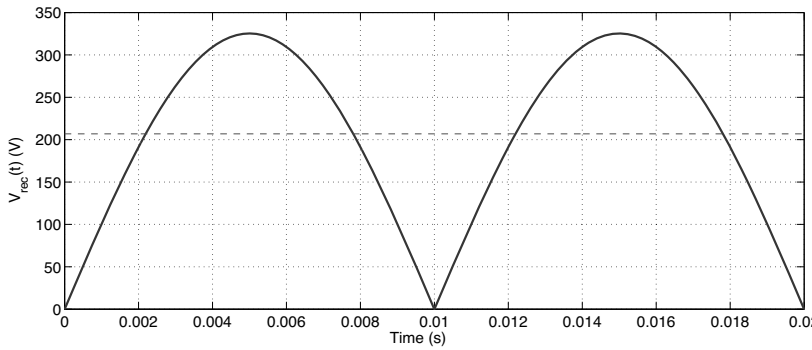


Figure 3.7. *Voltage waveforms for a half-wave single-phase rectifier*

When the rectifier powers a load modeled as a current source I_0 as shown in Figure 3.8, we see that the phase current i_a is expressed as:

- I_0 when V_{aN} is positive;
- $-I_0$ when V_{aN} is negative.

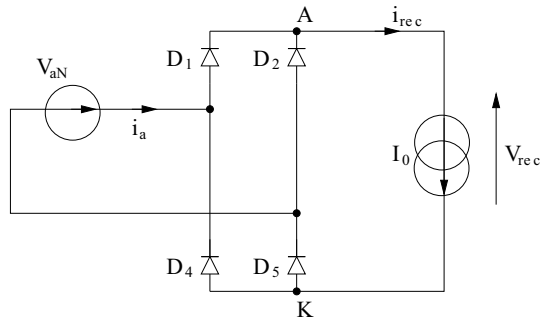


Figure 3.8. *Full-wave single-phase diode rectifier (*PD2*) with current source*

In this context, the evaluation of the input power factor λ_{PD2} of this bridge is trivial, as we can write the power P at the input and output of the converter as follows:

$$P = \langle V_{rec} \rangle .I_0 = \frac{2V_{\max}.I_0}{\pi} \qquad [3.19]$$

We may also write the apparent power S_e at the input of the rectifier, noting that $V_{\mathrm{RMS}} = V_{\max}/\sqrt{2}$ and $I_{\mathrm{RMS}} = I_0$. Hence:

$$\lambda_{\mathrm{PD2}} = \frac{P}{S_e} = \frac{2\sqrt{2}}{\pi} \simeq 0.900 \qquad [3.20]$$

The rectifier input current i_a is a square wave ($+I_0$ if $v_{aN} > 0$ and $-I_0$ if $v_{aN} < 0$), and consequently, it presents a fundamental component with an amplitude of $I_{a1\,\max} = \frac{4I_0}{\pi}$ in phase with the voltage provided by the network (i.e. an RMS value of $I_{a1\,\max} = \frac{2\sqrt{2}I_0}{\pi}$). From this, we conclude that the rectifier absorbs no reactive power, as the apparent power is simply composed of an active term and a distortion term ($S^2 = P^2 + D^2$).

For the three-phase PD3 full-wave bridge (see Figure 3.10), we note that the association of two P3 (one with

common cathodes, the other with common anodes) leads to an expression of the rectified average voltage $\langle V_{rec} \rangle$:

$$\langle V_{rec} \rangle = \frac{3V_{\max}\sqrt{3}}{\pi} \qquad [3.21]$$

This is a specific case of the general expression obtained for a bridge PDn:

$$\langle V_{rec} \rangle = \frac{2nV_{\max}}{\pi} \sin\left(\frac{\pi}{n}\right) \qquad [3.22]$$

The waveform of $V_{rec}(t)$ is shown in Figure 3.9 for the case of a power supply using a $230/400\,\mathrm{V}$ network at $50\,\mathrm{Hz}$.

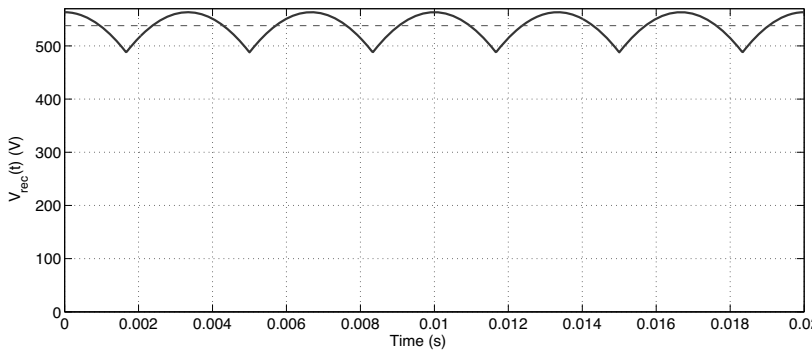


Figure 3.9. *Voltage waveforms for a PD3 diode rectifier*

Once again, we see that formula [3.22] is not directly applicable for the $\mathrm{PD2}$ bridge; as we have already seen, voltage V_{aN} is composed of two identical voltages in opposite phases, connecting the double single-phase bridge to those using greater numbers of phases.

The waveform obtained for a phase current with a "current source"-type load is presented in Figure 3.11. We see that, over a period, the current takes three distinct values ($+I_0$, 0 and $-I_0$) and that the signal is in phase with the voltage.

Consequently, the fundamental component of the current is purely active; no reactive power is consumed in the case of a PD3 diode rectifier (but a distortion power D exists).

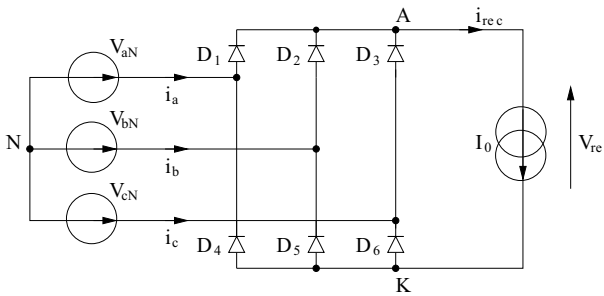


Figure 3.10. *Double-alternation three-phase diode rectifier (PD3) with current source*

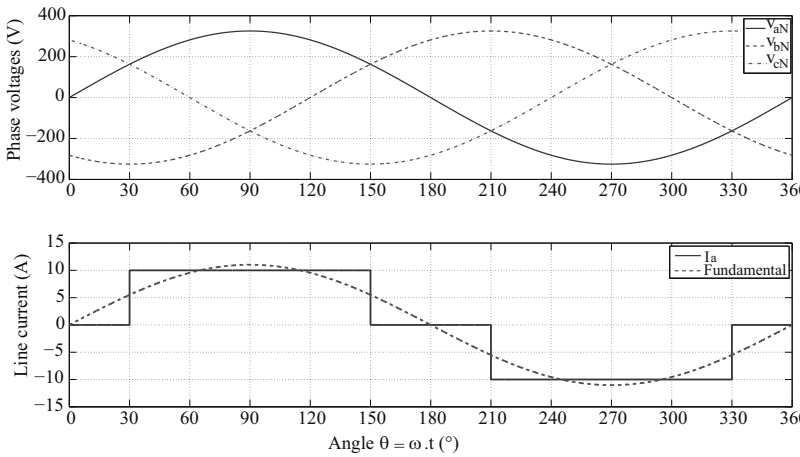


Figure 3.11. *Current waveforms for a PD3 diode rectifier. For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

Once again, we should consider the power factor at the input of this type of converter (PD3). To do this, we follow the

same method used above, calculating the active power output P:

$$P = \frac{3V_{\max}.I_0\sqrt{3}}{\pi} \quad [3.23]$$

We also calculate the apparent input power. To do this, we note that the currents absorbed in each phase are offset by 120°, and the currents are non-null for 2/3 of the period. For the phase current i_a (with a "current source I_0" type load, in accordance with Figure 3.10), we successively obtain:

– a null current for 1/6 of the period;

– a current equal to I_0 for 1/3 of the period;

– a null current again for 1/6 of the period;

– $i_a = -I_0$ for 1/3 of the period.

In this case, the RMS phase current $I_{a\mathrm{RMS}}$ is expressed as follows:

$$I_{a\mathrm{RMS}} = I_0.\sqrt{\frac{2}{3}} \quad [3.24]$$

We can then calculate the apparent power S at the rectifier input point:

$$S = 3V_{\mathrm{RMS}}.I_{a\mathrm{RMS}} = V_{\max} \cdot I_0.\sqrt{3} \quad [3.25]$$

From this, we deduce the corresponding power factor λ_{PD3}:

$$\lambda_{\mathrm{PD3}} = \frac{3}{\pi} \simeq 0.955 \quad [3.26]$$

We note that this power factor is better than that obtained using the full-wave single-phase bridge (PD2).

Considering only the fundamental component of the current, we note that this element has a maximum value $I_{a1\max}$ expressed as follows:

$$I_{a1\max} = \frac{4I_0}{\pi} \cos\left(\frac{\pi}{6}\right) = \frac{2\sqrt{3}I_0}{\pi} \quad [3.27]$$

giving an RMS value of $I_{a1\mathrm{RMS}} = \frac{\sqrt{6}I_0}{\pi}$.

3.2. Rectifier DC output filters

We will consider the dimensioning of a filter in the context of a PD2 rectifier, but this approach is applicable for all rectifier types, including controlled rectifiers (although the calculations involved are more complicated in the latter case).

3.2.1. *LC filters*

In the case of a rectifier (diode PD2, in this case) associated with an LC filter (see Figure 3.12), we note that:

– upstream, it behaves as a (quasi-) constant current source;

– downstream, it behaves as a (quasi-) constant voltage source.

We therefore consider from the outset that the LC filter obtains the desired objective (smoothing of the output voltage and the input current). This is a classic approach in power electronics (which will be seen again in the context of switch-mode power supplies in Volume 3 [PAT 15b]), used to ensure coherence between initial hypotheses and the results obtained with selected L and C values.

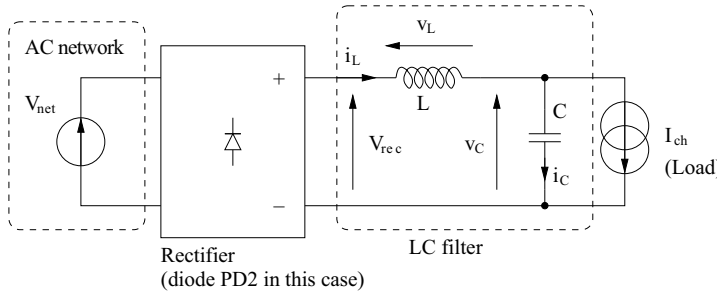


Figure 3.12. *LC filter at the output point of a rectifier*

In permanent mode, as the system evolves in a periodic manner ($100\,\text{Hz}$ for the output of a rectifier with a power supply of $50\,\text{Hz}$), we note that:

$$\langle v_L \rangle = 0 \qquad [3.28]$$

and:

$$\langle i_C \rangle = 0 \qquad [3.29]$$

If we consider that the current in the inductance is smooth and can be assimilated to a constant, the PD2 rectifier should behave in an identical manner to that shown in Figure 3.7.

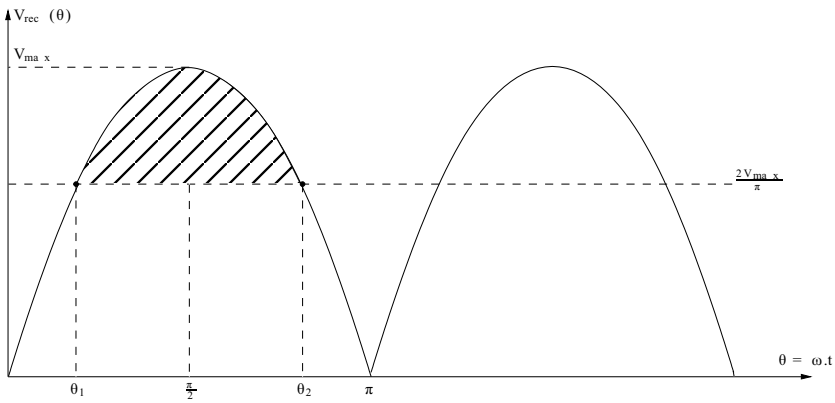


Figure 3.13. *Voltage waveforms for a full-wave rectifier*

In Figure 3.13, we see the average value of the voltage $V_{rec}(\theta)$ where $\theta = \omega.t$, along with the angles θ_1 and θ_2 at which the instantaneous voltage passes through this value during the interval $[0;\pi]$. These angles are defined as follows:

$$\theta_1 = \arcsin\left(\frac{2}{\pi}\right) \simeq 0.690\text{rad} = 39.5° \qquad [3.30]$$

and:

$$\theta_2 = \pi - \theta_1 \simeq 2.45\text{rad} = 140.5° \qquad [3.31]$$

If we take the voltage v_C at the capacitor terminals as constant, it can only be equal to $\frac{2V_{\max}}{\pi}$ as $\langle v_L \rangle = 0$, in accordance with the loop equation highlighted in Figure 3.12:

$$V_{rec} = v_L + v_C \qquad [3.32]$$

and thus:

$$\langle V_{rec} \rangle = \langle v_L \rangle + \langle v_C \rangle \qquad [3.33]$$

We can therefore calculate the peak-to-peak ripple ΔI_L of current i_L in the inductance:

$$\Delta I_L = \frac{1}{L\omega} \int_{\theta_1}^{\theta_2} V_{\max} \left(\sin\theta - \frac{2}{\pi}\right).d\theta \qquad [3.34]$$

By integration, we obtain:

$$\Delta I_L = \frac{V_{\max}}{L\omega} \left(-\cos\theta_2 + \cos\theta_1 - \frac{2}{\pi}(\theta_2 - \theta_1)\right) \qquad [3.35]$$

By symmetry in function $\cos(\cdot)$ and using the values of θ_1 and θ_2 established in equations [3.30] and [3.31], we may finally write that:

$$\Delta I_L = \frac{2V_{\max}}{L\omega} \left(\cos\theta_1 - 1 + \frac{2\theta_1}{\pi}\right) \simeq \frac{0,421V_{\max}}{L\omega} \qquad [3.36]$$

Once we have obtained this expression, we must simply define, for a given network (i.e. $V_{\max}$ and ω), the maximum acceptable level of current ripple in order to calculate the minimum required value of L.

For example, if we consider a $230\,V_{\mathrm{RMS}},\ 50\,\mathrm{Hz}$ network, and we know that the load consumes a current $I_{load} = 10\,\mathrm{A}$, we need to keep the current ripple in the inductance below $1\,\mathrm{A}$ from peak to peak (i.e. $10\,\%$ ripple). In these conditions, we obtain:

$$L = \frac{0.421 V_{\max}}{\Delta I_L \omega} \simeq 436\,\mathrm{mH} \qquad [3.37]$$

Note that this value is high for an inductance required to withstand a peak current of $10.5\,\mathrm{A}$ (without saturation[1]).

Once we have calculated the current ripple, we need to determine the expression of the peak-to-peak voltage ripple ΔV_C at the terminals of C. We know that the current i_L in the inductance includes a continuous component I_{L0} and a variable component δi_L:

$$i_L(\theta) = I_{L0} + \delta i_L(\theta) \qquad [3.38]$$

The current i_C in the capacitor only includes a variable component δi_C (as it has a null average value at steady state):

$$i_C(\theta) = \delta i_L(\theta) \qquad [3.39]$$

If the load absorbs a strictly constant current I_{load}, we deduce that:

$$I_{L0} = I_{load} \qquad [3.40]$$

1 In this type of application, we use an iron-core winding (see Chapter 5 [PAT 15a]).

and that the current ripple in the inductance is equal to the current in the capacitor:

$$\delta i_L = \delta i_C = i_C \qquad [3.41]$$

Several approaches may then be used to obtain the desired result (i.e. ΔV_C):

– accurate analytical calculation of the integral of δi_L (non-sinusoidal current);

– analytical calculation of the amplitude δI_{L1} of the fundamental component of current δi_L then of the corresponding ripple (limited to the harmonic) of voltage ΔV_{C1}, considered to be fairly close to ΔV_C;

– an approximate calculation based on the assumption that a sinusoidal ripple of current δi_L with a pulsation ω and a peak-to-peak amplitude ΔI_L will create a voltage ripple ΔV_C analogous to that obtained through accurate analytical calculations.

This final method provides satisfactory results for a very low number of calculations. It does not require us to integrate piecewise-defined sinusoidal signals or to calculate the fundamental component of a Fourier series. This method is therefore preferred in cases where a accurate result is not required (this is generally the case in practice).

The current ripple is fixed by the specification, so we may calculate the voltage ripple at the terminals of C by direct application of Ohm's (generalized) law:

$$\Delta V_C = \frac{\Delta I_L}{2C\omega} \qquad [3.42]$$

REMARK 3.2.– Note the presence of coefficient 2 in the denominator of this formula. As ω is the pulsation of the network, we must remember that the current (and voltage) ripple output from a PD2 diode rectifier will present a

pulsation (or frequency) of twice this value. In the case of a PD3 (still using diodes), a coefficient of 6 is required, as we see from the waveforms in Figure 3.9.

As for the current ripple (fixed at $1\,\mathrm{A}$ in our example), we determine a maximum value of ΔV_C in order to determine a minimum value of C. For example, we know that the output of a PD2 diode rectifier connected to a $230\,\mathrm{V_{RMS}},\ 50\,\mathrm{Hz}$ network will have an average voltage of $207\,\mathrm{V}$. We then need to select a maximum peak-to-peak ripple, for example $1\,\%$ (i.e. $2.07\,\mathrm{V}$) in order to obtain a result:

$$C = \frac{\Delta I_L}{2\Delta V_C \omega} \simeq \frac{1}{2 \times 2.07 \times 2\pi \times 50} = 769\,\mu\mathrm{F} \qquad [3.43]$$

3.2.2. *Capacitor filters*

While the solution presented above is effective in filtering terms, it is cumbersome and expensive due to the use of a coil. In low-cost approaches, we tend to prefer solutions which are satisfactory from a load perspective (good voltage filtering) but which do not perform as well from a source perspective (highly pulsed current in the network). This solution takes the form of a simple capacitor filter. In this configuration, as shown in Figure 3.14, a filtering capacitor is placed at the output terminals of the diode rectifier. In this section, we will consider the case of a PD2 diode rectifier. The network will be presumed ideal (zero impedance), as will the capacitor.

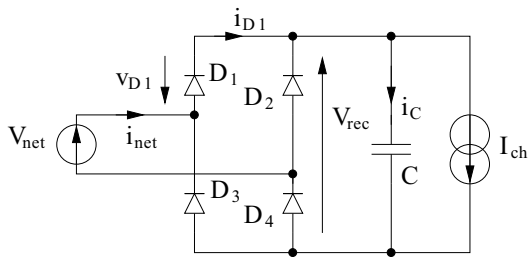


Figure 3.14. *Full-wave single phase rectifier with capacitor filter*

To simplify our study, we will also consider that the load behaves as an ideal current source, absorbing a current I_{load} independently of the applied voltage V_{rec}.

As in the case of operations with a load which behaves as a current source, the operating modes:

– mode 1: (D_1, D_4) ON and (D_2, D_3) OFF;

– mode 2: (D_1, D_4) OFF and (D_2, D_3) ON

are accessible; we also have an additional operating mode (mode 3) in which all of the diodes are switched off. In this specific case, the capacitor + source I_{load} assembly functions autonomously. This gives a constant current discharge, which consequently presents a linear reduction in voltage $V_{rec}(t)$ as a function of time:

$$V_{rec}\,(t) = -\frac{I_{load}t}{C} + V_{rec}\,(0) \qquad [3.44]$$

where $V_{rec}(0)$ is the initial voltage (at the beginning of this operating phase, we arbitrarily take $t = 0$).

It is also useful to change the variable in order to express this equation as a function of θ rather than t:

$$V_{rec}\,(\theta) = -\frac{I_{ch}\theta}{C\omega} + V_{rec}\,(0) \qquad [3.45]$$

Moreover, we see that when the rectifier is operating in mode 1 or mode 2, the voltage V_{rec} is always equal to $|V_{net}(t)|$. Consequently, a graphical representation (Figure 3.15) of the rectified value of the "network" voltage is useful as a basis for reasoning. Taking the hypothesis that the capacitor is fully discharged at the beginning of our study, and if $V_{net}(\theta) = V_{\max}.\sin(\theta)$, then the rectifier immediately switches to mode 1, and thus $V_{rec}(\theta) = V_{net}(\theta)$. This operating mode lies a little beyond angle $\theta = \frac{\pi}{2}$, and will be denoted as $\frac{\pi}{2} + \alpha$.

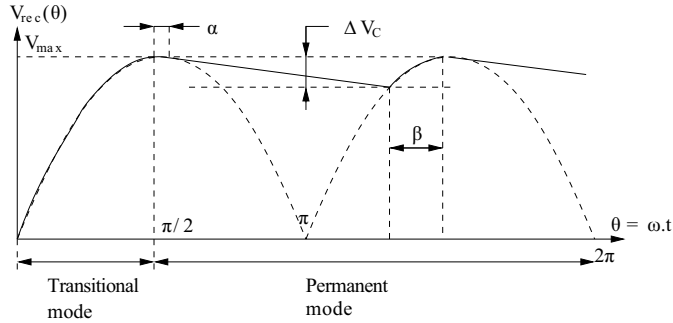


Figure 3.15. *Waveform for top capacitor filtering*

This angle, at which the rectifier switches to mode 3, corresponds to a cancellation of the current entering the rectifier. This current is equal to the sum $I_{ch} + i_C$. During the first operating phase (mode 1), we have:

$$i_C\,(t) = C\frac{dV_{rec}}{dt} \qquad [3.46]$$

and following θ with $V_{rec}\,(\theta) = V_{\max}.\sin\theta$:

$$i_C\,(\theta) = C\omega V_{\max}\cos\theta \qquad [3.47]$$

The current i_{net} is therefore canceled out when:

$$I_{load} + C\omega V_{\max}\cos\theta = 0 \qquad [3.48]$$

Replacing θ by $\frac{\pi}{2} + \alpha$, the previous equation becomes:

$$I_{load} - C\omega V_{\max}\sin\alpha = 0 \qquad [3.49]$$

i.e.:

$$\alpha = \arcsin\left(\frac{I_{load}}{C\omega V_{\max}}\right) \qquad [3.50]$$

REMARK 3.3.– Note that this angle is determined at the end of a phase in transitional mode, but it remains present in the following periods (i.e. in permanent mode).

The voltage at this instant constitutes the initial condition for operating mode 3:

$$V_{rec}\left(\theta = \frac{\pi}{2} + \alpha\right) = V_{\max}.\cos\alpha \qquad [3.51]$$

We then have a capacitor discharge in accordance with equation [3.45], and we need to determine angle β involved in the reestablishment of conduction through the rectifier (mode 2). The equation for the discharge line in the global reference frame is:

$$V_{rec}(\theta) = V_{\max}.\cos\alpha - \frac{I_{load}}{C\omega}\left(\theta - \frac{\pi}{2} - \alpha\right) \qquad [3.52]$$

We therefore need to calculate the angle of intersection $\frac{3\pi}{2} - \beta$ between this line and the equation of the sinusoid $-V_{\max}.\sin\theta$:

$$V_{\max}.\cos\alpha - \frac{I_{load}}{C\omega}\left(\frac{3\pi}{2} - \beta - \frac{\pi}{2} - \alpha\right) = -V_{\max}.\sin\left(\frac{3\pi}{2} - \beta\right) \qquad [3.53]$$

This may be rewritten as:

$$V_{\max}.\cos\alpha - \frac{I_{load}}{C\omega}(\pi - \alpha) = V_{\max}.\cos\beta - \frac{I_{load}}{C\omega}\beta \qquad [3.54]$$

This equation is hard to solve analytically. Evidently, a digital approach is entirely suitable (and simulations may be used in cases which are potentially more complex than for a "current source" type load), but we may also use simplifications if we assume that voltage smoothing is

effective (as for LC filtering). In these cases, angle β is low, and we may carry out a development of the cosine function:

$$\cos\beta \underset{0}{\sim} 1 - \frac{\beta^2}{2} \qquad [3.55]$$

We thus obtain:

$$V_{\max}.\cos\alpha - \frac{I_{load}}{C\omega}(\pi - \alpha) = V_{\max}.\left(1 - \frac{\beta^2}{2}\right) - \frac{I_{load}}{C\omega}\beta \qquad [3.56]$$

Note that α is no longer an unknown value, as we established an expression in [3.50]. The only unknown value is β, and the limited development allows us to establish a second-order equations. We thus see that when two real solutions are established, only one solution can genuinely be used; this solution must clearly lie within the interval $\left[0; \frac{\pi}{2}\right]$.

The simplest dimensioning approach is therefore iterative. It is best to fix a value for capacity *C* and evaluate the voltage ripple obtained in this case ($\Delta V_C = V_{\max}.(1 - \cos\beta)$), and then to adjust the value of C up or down as a function of the desired voltage ripple.

When selecting an initial capacity, we note that the phase of "mode 3" covers an angular range smaller than π radians; consequently, the voltage ripple ΔV_C cannot exceed the following value:

$$\Delta V_C = \frac{\pi I_{load}}{C\omega} \qquad [3.57]$$

As an example, if we consider a load consuming $10\,\mathrm{A}$ and a $230\,\mathrm{V_{RMS}},\ 50\,\mathrm{Hz}$ network, we may, for instance, initialize the dimensioning process using a voltage ripple of 10% (N.B. the value of the average output voltage is close to $V_{\max}$ and not to $\frac{2V_{\max}}{\pi}$ – we will therefore select a ripple ΔV_C of $32\,\mathrm{V}$). This choice leads us to select a capacitor value of $3,100\,\mu\mathrm{F}$.

Based on this choice, we can then calculate angles α and β:

$$\alpha = \arcsin\left(\frac{I_{ch}}{C\omega V_{\max}}\right) \simeq 0.031\text{rad} \quad [3.58]$$

giving us a very small angle (1.78°).

Once this result has been established, we can write our second-order equation in terms of β:

$$162.5\beta^2 + 10.27\beta - 32.1 = 0 \quad [3.59]$$

This equation has a positive discriminant $\Delta \simeq 20,970$ and therefore has two real roots, which we will call β_1 and β_2:

$$\beta_1 = \frac{-10.27 - \sqrt{\Delta}}{2 \times 162.5} \simeq -0.477\,\text{rad} \quad [3.60]$$

and:

$$\beta_2 = \frac{-10.27 + \sqrt{\Delta}}{2 \times 162.5} \simeq 0.414\text{rad} \quad [3.61]$$

We have already established a desired interval of $\left[0; \frac{\pi}{2}\right]$, i.e. approximately $[0; 1.57]$. We can therefore rule out angle β_1 and consider that the desired angle is $\beta_2 \simeq 0.414\,\text{rad} \simeq 23.7°$.

Finally, we may verify the voltage ripple value, knowing that $\Delta V_C = V_{\max}.(1 - \cos\beta)$. We obtain $\Delta V_C \simeq 27.5\,\text{V}$, representing an error of $5\,\text{V}$ in relation to the initial value used to calculate C with the "highly approximative" formula [3.57].

On this basis, we may create a graph of the current absorbed in the network (see Figure 3.16). A digital calculation of the fundamental component of this current gives us an amplitude of $20.6\,\text{A}$ ($14.56\,\text{A}_{\text{RMS}}$) and a phase shift of 15.3° in advance of the voltage. We can therefore evaluate the active power taken from the network ($3.24\,\text{kW}$). We can

also calculate the effective total current I_{net} ($31.75\,\mathrm{A_{RMS}}$) in order to deduce the apparent power ($7.3\,\mathrm{kVA}$). We thus obtain a very low-power factor (0.44) in comparison to that obtained using LC filtering, which can tend to the theoretical result obtained for a constant current source (0.9). Clearly, the benefits of this approach in terms of simplicity (and consequently, of cost savings) are most important in the case of "mass-market" low-power applications, although a large number of devices of this type connected to the network can have a significant effect on the network itself (and on the overdimensioning of all equipment, from power stations to the equipment used in the network).

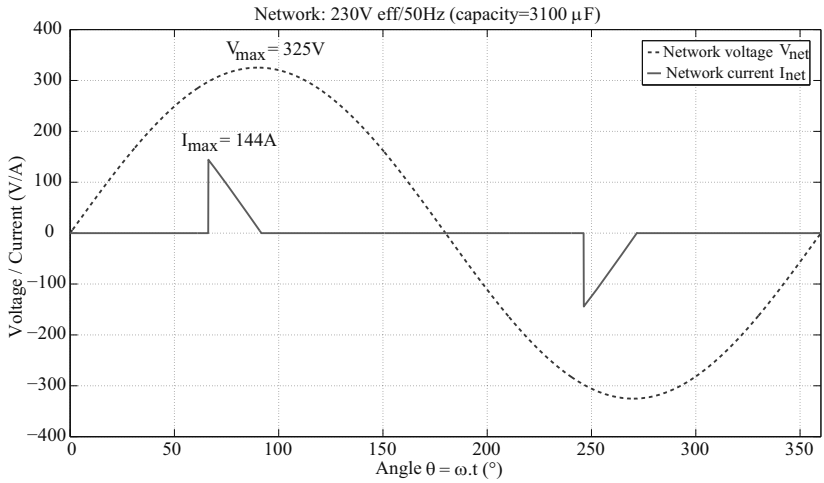


Figure 3.16. *Waveform for top capacitor filtering*

REMARK 3.4.– The result shown in Figure 3.16 corresponds to an ideal network. In practice, this current is somewhat smoothed (with no discontinuity when the bridge is switched) due to the impedance of the lines and transformers used in the electrical network. This reduces the distortion rate (which is still high) of the current I_{net}, and, as a result, slightly increases the input power factor of the rectifier.

3.3. Controlled rectification

3.3.1. *Half-wave bridges*

In studying controlled bridges, we begin by considering their uncontrolled equivalents, adding a delay in the conduction interval with a control angle ψ (the firing delay angle). This gives us rectified voltage V_{rec} waveforms with a higher level of ripple, but also, and especially, an average voltage $\langle V_{rec} \rangle$ which can be controlled using angle ψ (or, more accurately, $\cos \psi$).

Note that in theory, the value of ψ may vary from 0° to 180°; which means that $\cos \psi$ may take any value from 1 to -1 inclusive. In practice, the maximum accessible angle is approximately 150°. The remaining 30° are known as the buffer angle, and correspond to a time period of approximately $1.67\,\text{ms}$, which must be greater than or equal to the turn-off time (generally denoted as T_q) specified in manufacturer documentation. This corresponds to the minimum time needed to guarantee that the component will have regained the ability to switch off. If this time is not respected, the thyristor is switched back on, in the same way as a classic diode, when conditions are once again respected.

REMARK 3.5.– To use an analogy, we should remember that a thyristor is the electronic equivalent of a Water Closet (WC) flush system. The thyristor remains switched on as long as the current traveling through it is not canceled out; it only truly switches off when the current is canceled for a sufficient period of time (long enough to evacuate the charge stored in the semiconductor).

The P3 thyristor bridge has an average output voltage $\langle V_{rec} \rangle_{\text{P3}}$ of the form:

$$\langle V_{rec} \rangle_{\text{P3}} = \frac{3V_{\max}}{\pi} \sin\left(\frac{\pi}{3}\right) \cos \psi = \frac{3V_{\max}\sqrt{3}}{2\pi} \cos \psi \qquad [3.62]$$

In general terms, for a $\mathrm{P}n$ thyristor bridge, we have:

$$\langle V_{rec} \rangle_{\mathrm{P}n} = \frac{nV_{\max}}{\pi} \sin\left(\frac{\pi}{n}\right) \cos\psi \qquad [3.63]$$

At best, the power factor is equal to that of the corresponding diode bridge ($\psi = 0$), but is reduced as ψ increases. This is connected to the fact that the current wave is offset in relation to the voltage wave at the rectifier input terminals. In the case of diode rectifiers, the current fundamental was in phase with the sinusoidal voltage wave, and so we obtained $\cos\varphi_1 = 1$ (where φ_1 is the offset between the current fundamental and the voltage). The power factor was only degraded by the presence of a continuous component absorbed by the network, and by the multiple harmonics of the network voltage; this is known as a distorting power D. The reactive power Q was strictly null. In this case, the distortion power is still present, along with a non-null reactive power term, as $\varphi_1 = \psi$.

3.3.2. *Double bridges*

The control of "thyristor only" double bridges (PD2 or PD3, respectively, in Figures 3.17 and 3.18) allows them to provide a constant positive or negative voltage to a load, while the current in the load is unidirectional due to the unidirectional behavior of thyristors (which behave in the same way as diodes in this respect). The power supplied to the charge can therefore be positive or negative: the bridge either behaves as a rectifier, when power is directed from the *AC* side to the *DC* side, or as an inverter (assisted) when the power circulates from the *DC* side to the *AC* side. In this case, we talk of assisted inverters, as the bridge cannot operate as an inverter when the power is moving in the *AC* to *DC* direction: this operating mode corresponds to a braking mode, if the "*DC*" load is a DC electrical machine. From an application perspective, note that in this case, the powered machine will

operate in two quadrants (two directions of rotation, one torque direction); this corresponds to the case of a hoist or an elevator, for example.

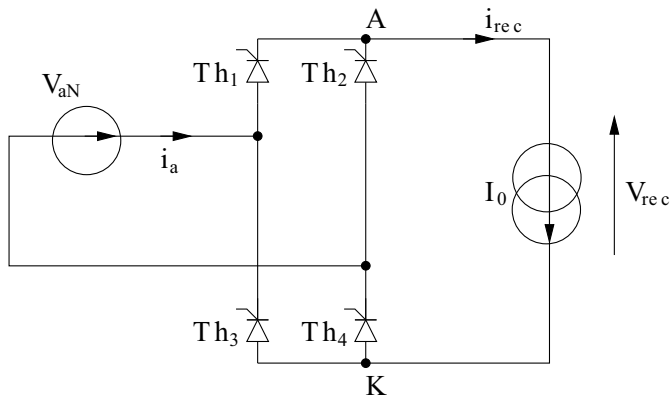


Figure 3.17. *Full-wave single-phase thyristor rectifier (PD2) with current source*

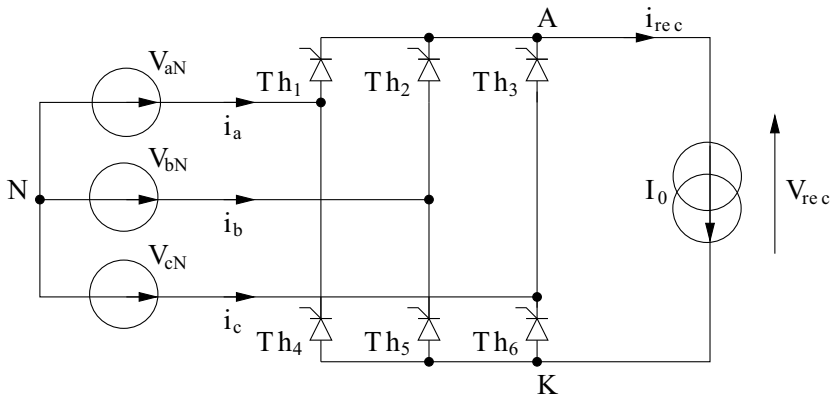


Figure 3.18. *Double-alternating three-phase thyristor rectifier (PD3) with current source*

As with half-wave bridges, the average output voltage of the rectifier takes the same expression as for non-controlled rectifiers (i.e. diode rectifiers), with the multiplication by a coefficient $\cos\psi$. In this case, for a PD3 bridge, we have:

$$\langle V_{rec}\rangle_{\mathrm{PD3}} = \frac{6V_{\max}}{\pi}\sin\left(\frac{\pi}{3}\right)\cos\psi = \frac{3V_{\max}\sqrt{3}}{\pi}\cos\psi \qquad [3.64]$$

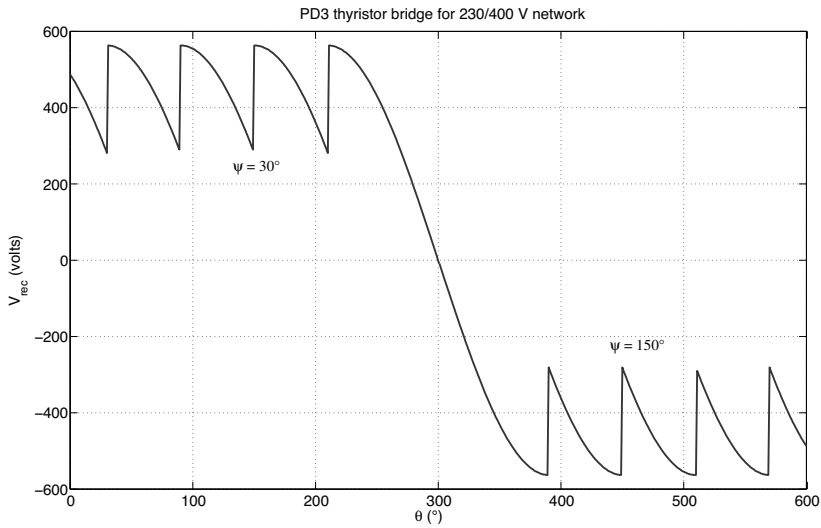


Figure 3.19. *Output voltage waveform for a PD3 thyristor rectifier ($\psi = 30°$ then $\psi = 150°$)*

More generally, for a PDn bridge:

$$\langle V_{rec}\rangle_{\mathrm{PD}n} = \frac{2nV_{\max}}{\pi}\sin\left(\frac{\pi}{n}\right)\cos\psi \qquad [3.65]$$

The current absorbed by a PD3 thyristor bridge is the same as that for a diode PD3, except for a phase shift of angle ψ in relation to the corresponding phase voltage, as shown in Figure 3.21.

We have the same expression for the maximum and effective values of the rectifier input current(s): this means that the apparent power is the same as for a diode rectifier, but with an offset of angle ψ between the voltage and the fundamental current (denoted as $i_{a1}(t)$). We therefore have the following active power:

$$P_{\mathrm{PD}n} = \frac{2nV_{\max}I_0}{\pi} \sin\left(\frac{\pi}{n}\right) \cos\psi \qquad [3.66]$$

and a reactive power of:

$$Q_{\mathrm{PD}n} = \frac{2nV_{\max}I_0}{\pi} \sin\left(\frac{\pi}{n}\right) \sin\psi \qquad [3.67]$$

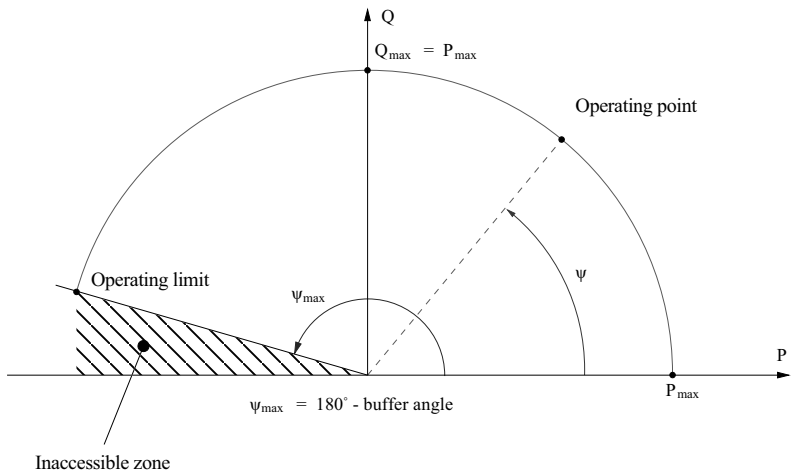


Figure 3.20. *Operating area of a PD3 thyristor bridge in the plane (P, Q) with current source*

In the specific case of a PD3 bridge, we have:

$$\begin{cases} P_{\mathrm{PD3}} = \frac{3V_{\max}I_0\sqrt{3}}{\pi} \cos\psi \\ Q_{\mathrm{PD3}} = \frac{3V_{\max}I_0\sqrt{3}}{\pi} \sin\psi \end{cases} \qquad [3.68]$$

We can then verify that $P^2 + Q^2 \neq S^2$, following the expression of S defined in [3.25] for the PD3 bridge (the result is valid for both diode and thyristor rectifiers). The apparent power S entering the rectifier therefore includes three components: the active power P, reactive power Q and distortion power D, in accordance with the relationship:

$$S^2 = P^2 + Q^2 + D^2 \qquad [3.69]$$

Note that this is the most general example of decomposition of the apparent power in non-sinusoidal periodic mode.

System [3.68] shows that the behavior of a PD3 thyristor bridge with a "current source I_0" type load may be represented in the plane (P, Q), located on a circle centered on the origin of the reference frame with a radius of $P_{max} = \frac{3V_{\max} I_0 \sqrt{3}}{\pi}$. Note that the area of possible operation is limited to the upper semi-circle, as illustrated by the graph in Figure 3.20; angles in excess of 150° are also generally inaccessible, due to the margin angle imposed by controls in order to provide thyristors with sufficient time to switch off.

The antiparallel connection of two full-wave three-phase thyristor bridges allows us to create a four-quadrant converter, each being responsible for two different quadrants. The control approach used may be more or less sophisticated, and may include the use of an interconnecting winding. These approaches include:

– control of one converter at a time (with non-instantaneous transition from one to the other when the current cancels out in the load – leading to momentary loss of control of the machine torque, in the case of a DC machine);

– simultaneous control of both converters, with a current circulating between the two (limited by circulating current inductor). While control is more complex in this case, there is no latency during the passage through zero current (no momentary loss of control).

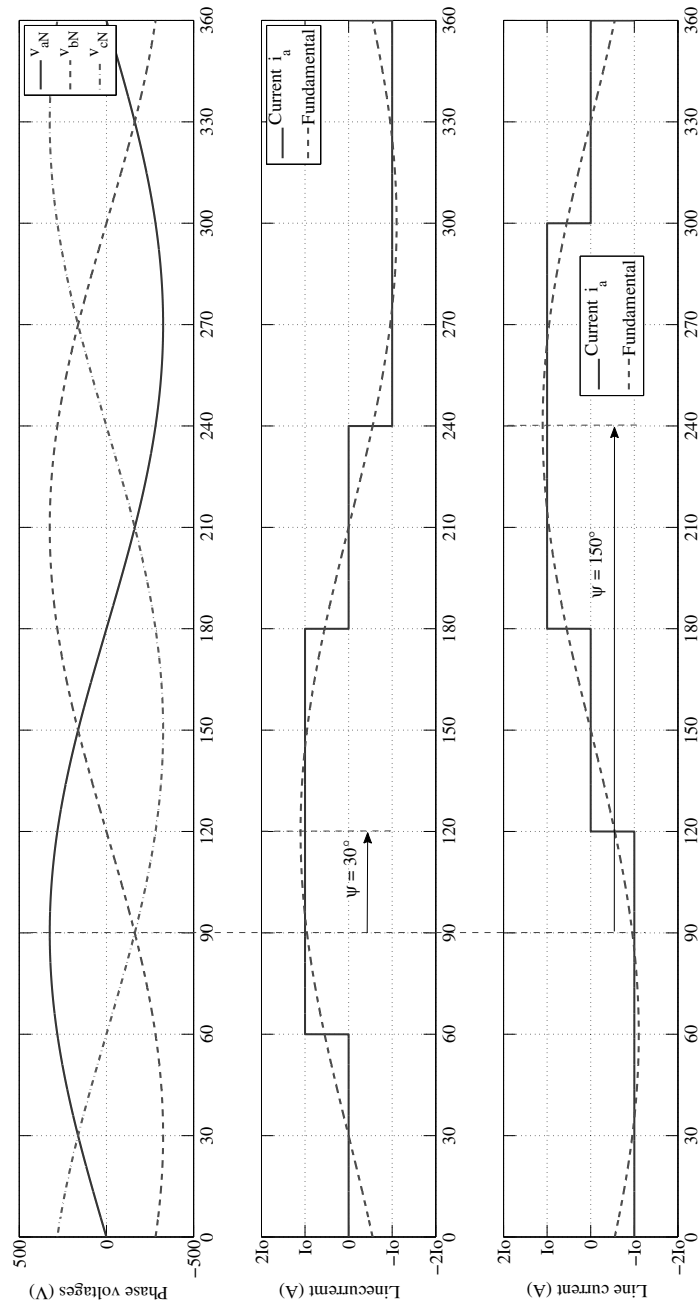


Figure 3.21. *Waveform of input line currents for a PD3 thyristor rectifier ($\psi = 30°$ then $\psi = 150°$). For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

3.3.2.1. *Half-controlled bridges*

Half-controlled PD2 and PD3 bridges are similar to the full-bridge thyristor versions, but half of the switches are diodes. In this case, we realize that the sign of the voltage supplied to the load can no longer be changed by controlling the thyristors. Therefore, only a strictly positive variable average voltage can be produced, hence these convertors are single-quadrant ones.

3.4. Overlap phenomenon

3.4.1. *Description and model*

So far, we have considered rectifiers connected to ideal voltage sources on the *AC* side and to ideal current sources on the *DC* side[2]. In practice, the AC sources used with rectifiers are not ideal voltage sources; they are, in fact, powerful networks characterized by an electromotive force electro-motive force (e.m.f.) in series with a low-value impedance. However, these networks notably include transformers, and, as seen in Chapter 5 of Volume 1 [PAT 15a], these components present a leakage inductance in their secondary winding (added to the line inductance of the cables separating a distribution transformer from the load). The input source can be modeled more accurately as a voltage source in series with an inductance (and even a resistance). In our specific context, however, we will ignore the resistance component of the network in order to focus on its inductive behavior. In rectifiers, this behavior is responsible for a phenomenon known as overlap.

This point may be illustrated using the specific example of a PD3 diode rectifier; we will then generalize our overlapping model for other converter types (diode or thyristor bridges). This study is based on the diagram shown in Figure 3.22,

2 With the exception of a rectifier with a capacitor filter.

where we see that in addition to e.m.f., the network presents identical inductances l_{net} for each phase (based on the hypothesis of a balanced network). However, the model of the DC bus is the same as that used in Figure 3.10: we consider that the load behaves as an ideal current source.

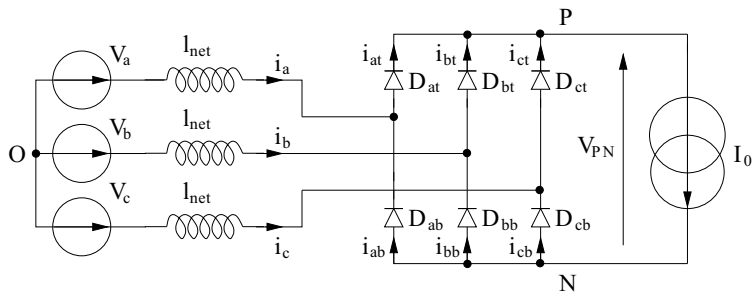


Figure 3.22. *Diode PD3 with a current-source type load, with input from an inductive network*

Having said that, it is no longer possible to switch from one diode to another in a switching cell. Previously, for the upper cell (D_1, D_2, D_3), for example, the conducting diode was the one having the highest potential at its anode. In this case, two diodes may be in conduction simultaneously; in fact when a diode begins to conduct (as the potential of its anode becomes higher than that of the diode previously in conduction), the current through it increases in a non-instantaneous manner, while the current in the diode which was initially in conduction decreases in the same proportion. The two currents (of diodes denoted as u and v, in the general case) must verify the following condition at all times:

$$i_u + i_v = I_0 \qquad [3.70]$$

As a consequence, the equation of a loop including two phases of the power network can be written:

$$V_u - V_v = l_{net}\left(\frac{di_u}{dt} - \frac{di_v}{dt}\right) \quad [3.71]$$

Based on [3.70]:

$$\frac{di_u}{dt} + \frac{di_v}{dt} = 0 \quad [3.72]$$

thus:

$$V_u - V_v = 2l_{net}\frac{di_u}{dt} \quad [3.73]$$

On the other hand, the input phase voltages V_u and V_v may be written in the form:

$$V_u = V_{\max}.\cos\left(\omega.t + \phi_0\right) \quad [3.74]$$

and:

$$V_v = V_{\max}.\cos\left(\omega.t + \phi_0 \pm \frac{2\pi}{3}\right) \quad [3.75]$$

These voltages consequently cross for:

$$\omega.t + \phi_0 = \pm\frac{\pi}{3} \quad [3.76]$$

having a value of $V_{\max}/2$.

Switching can then be analyzed from this instant (or, more accurately, this angle, after changing the variable $\theta = \omega.t + \phi_0$). Thus:

$$V_u = V_{\max}.\cos\left(\theta\right) \quad [3.77]$$

For V_v, we decide, arbitrarily, to consider that this voltage presents a lag[3]:

$$V_v = V_{\max}.\cos\left(\theta - \frac{2\pi}{3}\right) \qquad [3.78]$$

Consequently, before $\theta_0 = \pi/3$, the conducting diode is D_{ut}; after this instant, diode D_{vt} enters into conduction. It is therefore necessary to evaluate the duration of simultaneous conduction in the two diodes (known as overlap). Taking equation [3.73], after changing the variable, we may write:

$$i_u(\theta) - i_u(\theta_0) = \frac{1}{2l_{net}\omega}\int_{\theta_0}^{\theta}\left(V_u(\xi) - V_v(\xi)\right).d\xi \qquad [3.79]$$

As diode D_{ut} is in conduction before θ_0, we know that $i_u(\theta_0) = I_0$. Replacing V_u and V_v by their expressions, we obtain:

$$i_u(\theta) = I_0 + \frac{V_{\max}}{2l_{net}\omega}\cdot\int_{\theta_0}^{\theta}\left(\cos(\xi) - \cos\left(\xi - \frac{2\pi}{3}\right)\right).d\xi \qquad [3.80]$$

hence:

$$i_u(\theta) = I_0 + \frac{V_{\max}}{2l_{net}\omega}\cdot\left[\sin(\theta) - \sin(\theta_0) + \sin\left(\theta_0 - \frac{2\pi}{3}\right) - \sin\left(\theta - \frac{2\pi}{3}\right)\right] \qquad [3.81]$$

Taking $\theta_0 = \pi/3$, we obtain:

$$i_u(\theta) = I_0 + \frac{V_{\max}}{2l_{net}\omega}\cdot\left[\sin(\theta) - \sin\left(\theta - \frac{2\pi}{3}\right) - 2\sin\left(\frac{\pi}{3}\right)\right] \qquad [3.82]$$

3 This choice does not affect the final result.

Finally, as we like to consider an instant θ situated after θ_0, we can change the variable again:

$$\theta = \theta_0 + \alpha = \frac{\pi}{3} + \alpha \qquad [3.83]$$

Hence:

$$i_u(\theta) = I_0 + \frac{V_{\max}}{2l_{net}\omega} \cdot \left[\sin\left(\frac{\pi}{3} + \alpha\right) - \sin\left(\alpha - \frac{\pi}{3}\right) - 2\sin\left(\frac{\pi}{3}\right)\right] \qquad [3.84]$$

We may use this result with the following trigonometric formulas:

$$\begin{cases} \sin(a+b) = \sin a.\cos b + \sin b.\cos a \\ \sin(a-b) = \sin a.\cos b - \sin b.\cos a \end{cases} \qquad [3.85]$$

hence:

$$i_u\left(\theta = \frac{\pi}{3} + \alpha\right) = I_0 - \frac{\sqrt{3}V_{\max}}{2l_{net}\omega} \cdot (1 - \cos\alpha) \qquad [3.86]$$

The "angular" duration $\alpha = \alpha_e$ of simultaneous connection of the two diodes can then be calculated by determining the instant at which current i_u cancels out:

$$i_u\left(\frac{\pi}{3} + \alpha_e\right) = I_0 - \frac{\sqrt{3}V_{\max}}{2l_{net}\omega} \cdot (1 - \cos\alpha_e) = 0 \qquad [3.87]$$

We thus obtain:

$$1 - \cos\alpha_e = \frac{2l_{net}\omega.I_0}{\sqrt{3}V_{\max}} \qquad [3.88]$$

hence:

$$\alpha_e = \arccos\left(1 - \frac{2l_{net}\omega.I_0}{\sqrt{3}V_{\max}}\right) \qquad [3.89]$$

During the phase in question, we may calculate the voltage v_{PO} applied to the common anode of the rectifier:

$$v_{PO} = V_u - l_{net}\frac{di_u}{dt} = V_v - l_{net}\frac{di_v}{dt} \quad [3.90]$$

hence:

$$v_{PO} = \frac{1}{2}\left(V_u - l_{net}\frac{di_u}{dt} + V_v - l_{net}\frac{di_v}{dt}\right) \quad [3.91]$$

and, using [3.72], we can simplify this expression to obtain:

$$v_{PO} = \frac{1}{2}\left(V_u + V_v\right) \quad [3.92]$$

As voltage V_v becomes higher than V_u, the obtained voltage is lower than that used in the idealized model presented above. Thus, overlap leads to an instantaneous voltage drop-off, resulting in a reduction in the average voltage over a period. As we have already seen, the average output voltage of a double bridge is twice the voltage of a single bridge. This is still verifiable, so we may base our reasoning on the single bridge (D_{1t},D_{2t},D_{3t}). We may calculate the average voltage $\langle v_{PO}\rangle$, placing the overlap phase at the beginning of the integration interval. In our case, we like to integrate $v_{P0}(\theta)$ between $\pi/3$ and π:

$$\begin{aligned}\langle v_{PO}\rangle = \tfrac{2\pi}{3}\int_{\pi/3}^{\pi} v_{PO}\left(\theta\right).d\theta = \tfrac{2\pi}{3}\Big(&\int_{\pi/3}^{\pi/3+\alpha_e}\tfrac{V_u(\theta)+V_v(\theta)}{2}d\theta \\ &+ \int_{\pi/3+\alpha_e}^{\pi} V_v\left(\theta\right).d\theta\Big)\end{aligned} \quad [3.93]$$

remembering that:

$$\begin{cases} V_u\left(\theta\right) = V_{\max}.\cos\left(\theta\right) \\ V_v\left(\theta\right) = V_{\max}.\cos\left(\theta - \frac{2\pi}{3}\right) \end{cases} \quad [3.94]$$

In order to simplify the calculation, it is useful to determine the voltage drop-off resulting from the overlap and

not the expression of the output voltage. We therefore need to calculate the difference between the ideal average output voltage, denoted as $\langle v_{PO} \rangle_0$, and [3.93]. Note that:

$$\begin{aligned}\langle v_{PO} \rangle_0 &= \frac{2\pi}{3} \int_{\pi/3}^{\pi} V_v(\theta) .d\theta \\ &= \frac{3}{2\pi} \left(\int_{\pi/3}^{\pi/3+\alpha_e} V_v(\theta) \, d\theta + \int_{\pi/3+\alpha_e}^{\pi} V_v(\theta) .d\theta \right)\end{aligned} \quad [3.95]$$

hence:

$$\begin{aligned}\Delta \langle v_{PO} \rangle &= \langle v_{PO} \rangle - \langle v_{PO} \rangle_0 \\ &= \frac{3}{2\pi} \left(\int_{\pi/3}^{\pi/3+\alpha_e} \frac{V_u(\theta) - V_v(\theta)}{2} d\theta \right)\end{aligned} \quad [3.96]$$

Replacing V_u, V_v and α_e by their respective values, we obtain:

$$\begin{aligned}\Delta \langle v_{PO} \rangle &= \frac{3V_{\max}\sqrt{3}}{4\pi} \\ &\times \left(\int_{\pi/3}^{\pi/3+\arccos\left(1-\frac{2l_{net}\omega.I_0}{\sqrt{3}V_{\max}}\right)} \cos\left(\theta + \frac{\pi}{6}\right) d\theta \right)\end{aligned} \quad [3.97]$$

hence:

$$\begin{aligned}\Delta \langle v_{PO} \rangle &= \frac{3V_{\max}\sqrt{3}}{4\pi} \\ &\times \left(\sin\left(\frac{\pi}{2} + \arccos\left(1 - \frac{2l_{net}\omega.I_0}{\sqrt{3}V_{\max}} \right) \right) - 1 \right)\end{aligned} \quad [3.98]$$

Applying one of the trigonometric formulas set out in [3.85], we obtain:

$$\Delta \langle v_{PO} \rangle = -\frac{3l_{net}\omega.I_0}{2\pi} \quad [3.99]$$

There is clearly a voltage drop-off, which is demonstrated by the "-" sign. Furthermore, we see that this voltage drop-off is proportional to the current supplied to the load. Consequently, the system behaves as if this drop-off resulted from a resistance: this is known as the equivalent overlap resistance

This result corresponds to a half-wave bridge. We note that the voltage drop-off is doubled for a full-wave bridge. The result can be generalized for any number k of phases (for half-wave bridges Pk and full-wave bridges PDk):

$$\begin{cases} \Delta \langle v_{PN} \rangle_{Pk} = -\frac{kl_{net}\omega.I_0}{2\pi} \\ \Delta \langle v_{PN} \rangle_{PDk} = -\frac{kl_{net}\omega.I_0}{\pi} \end{cases} \quad [3.100]$$

The equivalent overlap resistances are thus R_{emp}^{Pk} and R_{emp}^{PDk}, respectively, defined as follows:

$$\begin{cases} R_{emp}^{Pk} = \frac{kl_{net}\omega}{2\pi} \\ R_{emp}^{PDk} = \frac{kl_{net}\omega}{\pi} \end{cases} \quad [3.101]$$

REMARK 3.6.– While these results have been obtained for diode bridges, they can also be transposed to controlled rectifiers.

3.4.2. *Other rectifier voltage drop-offs*

We have seen that overlap leads to a voltage drop-off which may be assimilated to a resistance. This should not be confused with other potential resistive drop-offs which may occur at the input and output points of the rectifier as a result of the real resistances present in the cables. These drop-offs therefore need to be added. Finally, in a fine model of a rectifier, we need to take account of the voltage drop-offs introduced by diodes in the ON state. In practice, these may be assimilated to quasi-ideal voltage sources (V_F of the

diode). In the case of single bridges, where a single diode is in a state of conduction, we simply have a drop-off of V_F in the rectifier output; for double bridges, two diodes are involved, and the drop-off is therefore $2V_F$.

3.5. Association of rectifier assemblies

3.5.1. *Parallel associations and interphase windings*

3.5.1.1. *Half-wave bridges and applications*

Parallel associations are important in low-voltage, high-current applications, such as in electrochemical factories (e.g. the electrolysis troughs used in aluminum production). In this case, half-wave bridges are preferred in order to minimize voltage drop-offs (in steady state, a voltage drop-off at the terminals of a single switch, instead of two switches in a full-wave bridge, is observed); however, it is essential to reduce the current in the switches, as there are no component units able to process the current required by the load.

It is therefore necessary to interconnect two (or more) converters, which operate in parallel, and each supply a current of $I_0/2$ (or less) to provide a total current of I_0 to the load. This interconnection involves the use of two half-windings (as in the association of full-wave bridges shown in Figure 3.23) in order to smooth the currents, notably the ripple δi, known as circulation current, which travels from one converter to the other due to the differential voltage ripple produced by the two converters (e.g. the two rectifiers are powered by three-phase systems, offset by 60°). These two half-windings are both crossed by a very high current ($I_0/2$), with the addition of a ripple δi, which we reduce by choosing a suitable global inductance value L (for the two half-windings). To avoid overdimensioning the half-windings, the two components are produced using a common magnetic circuit, taking care to compensate the ampere turns linked to the two currents $I_0/2$. This may be referred to as a common mode, where the currents leave from

the same point (the middle of the winding assembly) to travel toward the load. Thus, the (non-saturated) magnetic circuit is dimensioned for the "small" circulation current, δi, alone.

REMARK 3.7.– However, the windings (copper) must clearly be dimensioned in order to withstand the full current.

This assembly must be produced with care, using components of the same type placed on the same heat sink (in order to guarantee use at the same temperature, or at least the closest possible temperature). The connections must be perfectly symmetrical. Under these conditions, the currents between the two converters should balance "naturally". However, the use of uncontrolled rectifiers is not recommended, and it is better to use two current rectification mechanisms (see [COH 00] on automatics) for the currents in the two converters, enabling us to use controls in order to force balancing of the currents if differences remain.

REMARK 3.8.– This type of technique is not limited to rectifiers, and is also used for choppers using low voltages and high currents. In this case, we speak of interleaved choppers. This type of converter is widely used to power central processing unit (CPU) (or graphics processing unit (GPU)) cores in computers; they are powered by a voltage of approximately 1 V, and consume a power of several tens of watts (or more). The currents involved are therefore high, and components with a very low-voltage drop-off are needed in order to obtain satisfactory efficiency (the term *synchronous rectifier* is often used). These components are used in parallel associations with balanced currents. Note, however, that the primary reason for using interleaved choppers for very low-voltage, high-current power supplies, for microprocessors and other high-density digital circuits very large scale integration (VLSI), is their ability to provide a very rapid response time for voltage regulation, due to sudden and drastic variations in consumption by the load.

3.5.1.2. *Full-wave bridges and "four-quadrant" drives*

In order to power a DC machine using all four quadrants (in motor or generator mode, with two possible directions of rotation), two full-wave thyristor bridges are needed, placed top to tail, as shown in Figure 3.23 for two PD3 type bridges (PD2 bridges may also be used for this purpose). Note that in this figure, the two bridges are connected to a machine (on the DC side) via an interphase winding, as seen in the previous section.

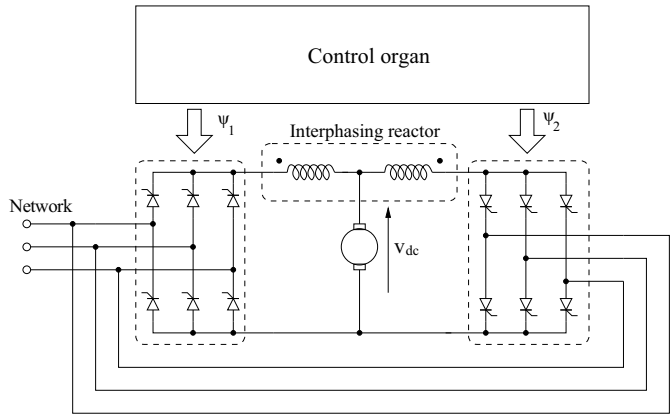


Figure 3.23. *Four-quadrant thyristor converter*

The latter component is optional in this case, but provides improved dynamic performance. Using this element, the two converters operate simultaneously, allowing the transition "$v_{dc} > 0$" → "$v_{dc} < 0$» (or vice versa) to occur seamlessly. In a configuration without this winding, bridges where "$v_{dc} > 0$" and "$v_{dc} < 0$" are used successively, and a deadtime needs to be included in the inversion logic used for global control in order to ensure secure transition for the converter.

The choice between these two solutions is made based on the following criteria:

– weight/space requirements of the winding;

– additional cost due to the winding;

– complexity of control (inversion logic in the winding-free configuration[4]);

– dynamic constraints of the application in mechanical terms: are rapid changes to the direction of rotation required?

This final point is fundamental in the choice of any converter used to power a DC machine, as it is always possible to use a mechanical switch for the polarity inversion function (changing the direction of rotation). This solution is simple, robust and economical, and should not be ignored during the design process, as it is largely sufficient in a considerable number of cases.

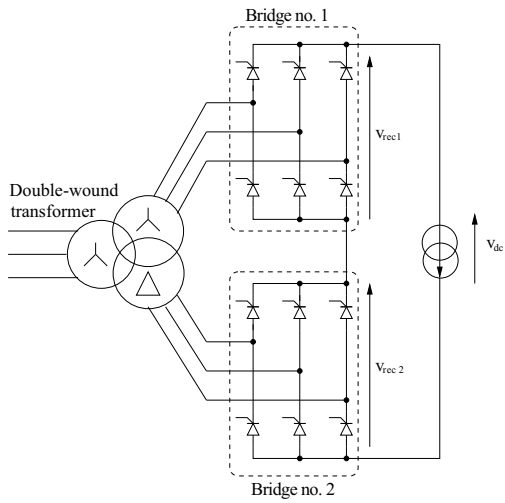


Figure 3.24. *Series association of two thyristor PD3s*

3.5.2. *Series association*

The series association of rectifier assemblies (see Figure 3.24) is the "dual" of the parallel association. While parallel association is used for applications with high current

4 The version of the structure including winding is, in fact, simpler.

values (with the exception of the four-quadrant configuration seen above), series association is used for high voltages. The best-known example of this type is in the transportation of DC energy. Electrical energy is always carried over long distances at high voltages, as since $P = U.I$ (with the addition of a coefficient dependent on the power supply type), at a given power, high voltages lead to low currents. This makes it possible to reduce the diameter of cables (although the insulation between the cables needs to be reinforced, this is lighter and less expensive).

REMARK 3.9.– The transportation of DC energy involves the use of generating stations, where converters are used as rectifiers; the opposite stations operate as inverters (assisted inverters, in the case of thyristors). Converters are associated in a four-quadrant configuration as shown in Figure 3.25, to ensure continuous current circulation in DC links. This structure is close to that shown in Figure 3.23.

The two PD3 bridges in the converter shown in Figure 3.24 can be controlled independently. This means that an infinite number of control strategies are possible. However, offset control of phase angles (denoted as ψ_1 and ψ_2 for the two bridges) is preferred due to the power factor, as shown in the graph of Figure 3.26 (a trace which leaves out the buffer angles). In Figure 3.20, we saw that a rectifier absorbs an "active power P/reactive power Q" element, which describes a circle in the plane (P, Q) as a function of the control angle. Consequently, in the case of common angle control (ψ_1=ψ_2), a large circle is produced; if the two angles are controlled separately with an offset, we expect to produce two small circles, minimizing the reactive power. In theory, this allows us to divide the reactive power taken from the network by 2 using offset control of the two bridges. In practice, the buffer angles of the two rectifiers mean that this gain is reduced; however, it is not negligible, particularly in the case of high-power applications.

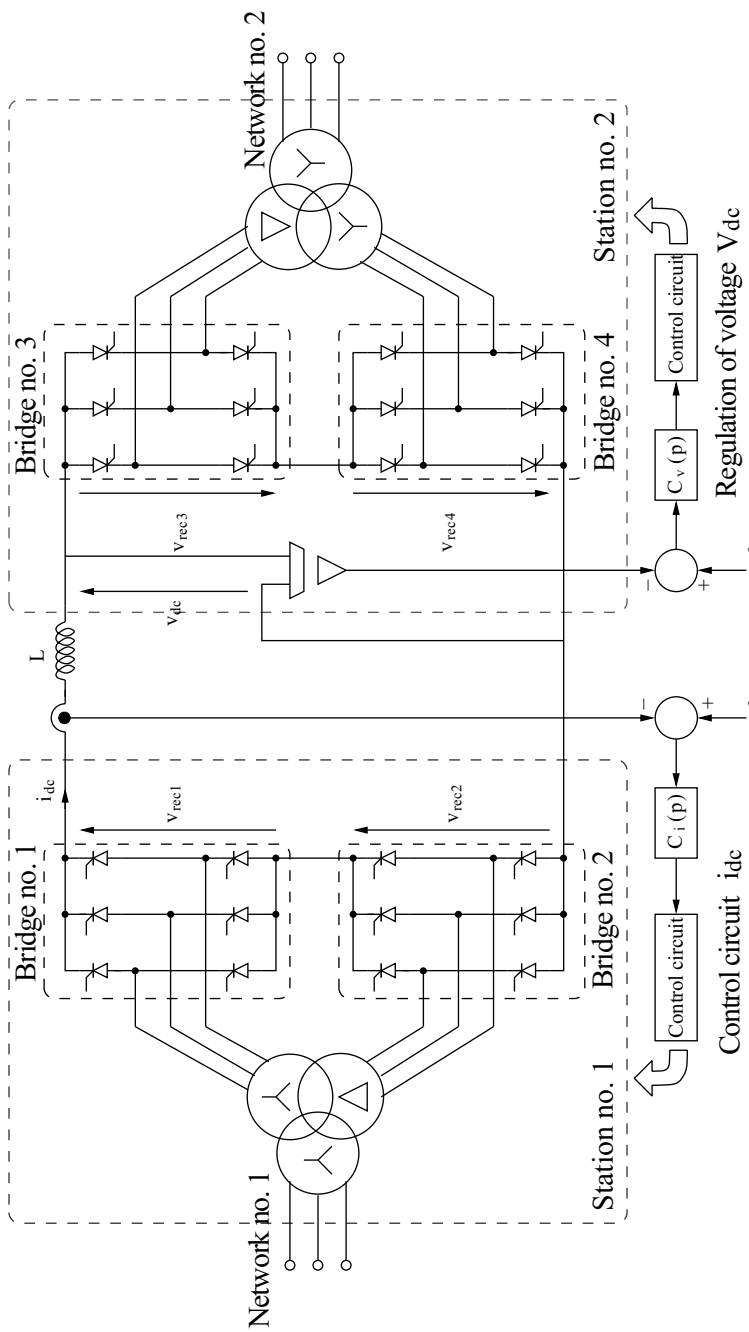


Figure 3.25. *DC link between two alternating networks*

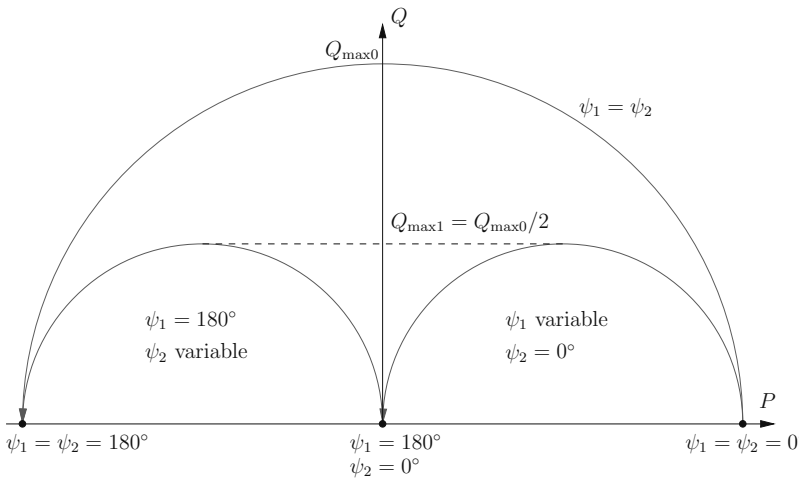


Figure 3.26. *Operating area of the series association of two PD3 thyristor bridges in the plane* (P, Q) *with a current source*

3.6. Power factor correction

3.6.1. *Single-phase PWM rectifier*

The single-phase inverter presented in Chapter 2 is potentially power-reversible, and can act as a rectifier. Note the presence of the four free-wheel diodes, which (if the four transistors are not controlled) constitute a double single-phase PD2 bridge; however, the interest of this converter in rectifier mode lies in the presence of transistors which permit significant gains in terms of the power factor, providing sinusoidal current input on the *AC* side. The payoff for this gain is an increase in complexity. This type of converter also enables significant levels of energy recuperation during braking phases. They are notably used in rail traction, in locomotives such as the BB36000 (as shown in Figure 3.27).

Figure 3.27. *BB36000 locomotive*

3.6.2. *Three-phase rectifier*

In the case of a three-phase rectifier, it is entirely reasonable to use a three-phase transistor bridge for sinusoidal current input. However, the gain in terms of the power factor is reduced, and is only limited by the harmonic pollution standards applicable to the network (and more generally by electromagnetic compatibility issues in the created equipment). This solution is rarely used, despite the fact that its power reversibility properties during braking lead to energy savings (there is no need for a braking chopper, and no energy needs to be dissipated as heat in a resistor). It should be noted, however, that this type of structure can only effectively return energy to the network (and thus slow down a mechanical load) if the network is operational. If a fault occurs leading to a switch being flipped further back in the circuit, the element will no longer be able to brake. In this case, a rheostatic (chopper and braking resistance) and/or mechanical braking system is required, and must always be included as backup for safety reasons.

3.6.3. *Single-phase rectifier without power reversal*

In applications where power reversibility is not required, a diode rectifier may be used as the application input module (in this case, we will consider a single-phase context with a PD2 diode bridge). We therefore need to know whether sinusoidal current input may be achieved by placing an appropriate (and suitably controlled) converter between the rectifier and the powered *DC* load. As a *DC* source is being connected to a *DC* load, a DC/DC converter is clearly required.

Qualitatively speaking, sinusoidal input is obtained as long as the load associated with the converter behaves in the same way as an equivalent resistance. Thus, the voltage $v_{rec}(t)$ entering the DC/DC converter (or exiting the rectifier) is expressed as follows:

$$v_{rec}\,(t) = V_{\max}.\,|\cos\,(\omega t + \varphi)| \qquad [3.102]$$

The voltage output from the DC/DC converter must be quasi-constant ($v_s(t) = V_s = \mathrm{Cte}$). If the application requires $V_s > 0$[5], two distinct possibilities are obtained:

– $V_s < V_{\max}$: the converter may operate by increasing or reducing the voltage;

– $V_s > V_{\max}$: the converter can only increase the voltage.

In the first case (if the structure is not galvanically isolated), an inductive storage chopper, known as a *buck-boost converter*, is used. This converter type will not be discussed further in this chapter, but will be covered in Chapter 4. In this section, we will focus on the second possible case, involving a parallel chopper, which is known as a *boost converter*. Both types of converter implicated in this specific context are known as *power factor correctors* (PFCs).

5 This arbitrary choice in no way limits the general nature of our study.

3.6.3.1. *Boost study*

In the case of the boost converter (Figure 3.28), with $V_e = v_{rec}(t)$, the output voltage can be shown to be always greater than or equal to the input voltage, whatever the value of the duty ratio α used to control the transistor T.

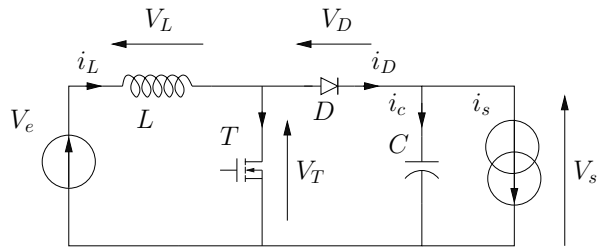


Figure 3.28. *Diagram of a boost converter*

DC control is preferred for this type of converter. We may study the converter by splitting the switching period T_d as before (but considering, in this case, that $i_L(0) \neq 0$).

Hence, for $0 \leq t < \alpha T_d$:

$$V_T = 0 \qquad [3.103]$$

and thus:

$$V_L = V_e \qquad [3.104]$$

leading to (for a current $i_L(0) = I_{L\min}$):

$$i_L(t) = I_{L\min} + \frac{V_e}{L}t \qquad [3.105]$$

In addition:

$$V_d = V_e - V_s \qquad [3.106]$$

Hence, for this booster assembly (see the full study in Chapter 1 of Volume 3 [PAT 15b]), $V_s > V_e$, and therefore $V_d < 0$. Consequently, the diode is switched off:

$$I_d = 0 \qquad [3.107]$$

With a voltage of V_s (presumed to be quasi-constant), the capacitor C discharges in order to power the load connected to the converter output:

$$I_s = -I_c \qquad [3.108]$$

Next, considering the second phase of the switching period (for $\alpha T_d \leq t < T_d$), where transistor T is open:

$$I_T = 0 \qquad [3.109]$$

The continuity of the current in the inductance L means that the diode enters into conduction, with an initial current equal to $i_L(\alpha T_d) = I_{L\max}$:

$$i_{L\max} = I_{L\min} + \frac{\alpha T_d V_e}{L} \qquad [3.110]$$

As diode $V_d = 0$ enters into conduction, then:

$$V_L = V_e - V_s < 0 \qquad [3.111]$$

and:

$$I_d = i_L = I_c + I_s \qquad [3.112]$$

Clearly, as $V_L < 0$, current i_L decreases to return to $I_{L\min}$ (as ever, our study is based on the converter operating in permanent mode). One consequence of this hypothesis is that, classically:

$$\langle V_L \rangle = 0 \qquad [3.113]$$

and as:

$$\langle V_L \rangle = \frac{1}{T_d} \left(V_e \alpha T_d + (V_e - V_s) \,.\, (1 - \alpha)\, T_d \right) \qquad [3.114]$$

the following result is deduced:

$$V_s = \frac{V_e}{1 - \alpha} \qquad [3.115]$$

This converter therefore increases the voltage, whatever the value of a (extreme case: $V_s = V_e$ for $\alpha = 0$).

However, to ensure rectification with sinusoidal input, a deeper study should be apprehended, presuming that sinusoidal input (in phase with the voltage $V_e(t) = V_{e\max} . |\sin(\omega t)|$) is achieved: this gives a fluctuating power $P(t)$ entering the converter:

$$P(t) = \frac{V_{e\max} . I_{e\max}}{2} \left(1 - \cos(2\omega t)\right) \qquad [3.116]$$

The power taken from a 50 Hz network therefore fluctuates at 100 Hz. To maintain a quasi-constant voltage output from the converter, a high-value capacitor C is required. Assuming that the output voltage is strictly constant (negligible ripple, in particular for the component at 100 Hz), the output power (P_s), presumed to be constant, is equal to the average input power.

Taking P_s as the input value for our problem, the following expression of $I_{e\max}$ can be used:

$$I_{e\max} = \frac{2P_s}{V_{e\max}} \qquad [3.117]$$

From this, the "low-frequency" voltage at the terminals of the inductance L in the boost converter may be deduced:

$$L \frac{di_L}{dt} = L \frac{d}{dt} \left[I_{e\max} . |\cos(\omega t + \varphi)| \right] \qquad [3.118]$$

The dimensioning of the inductance L is generally based on a current ripple rate required by the specification (e.g. 10% of the maximum value). On this basis, knowing the values of L, $I_{e\max}$ and ω, we see that the voltage v_T becomes negative for time intervals in the vicinity of instants where the converter input voltage V_e cancels out.

This is illustrated by the "low-frequency" waveforms as shown in Figure 3.29. These traces were obtained for a $230\,\text{V}/50\,\text{Hz}$ network with an inductance of $1\,\text{mH}$ and an input current with an amplitude of $1\,\text{A}$. Polarity reversal in the transistor is impossible in practice, in particular for a MOSFET transistor (with integrated anti-parallel diode): this leads to a slight loss of control over the converter, with a subsequent slight distortion of the input current at these instants.

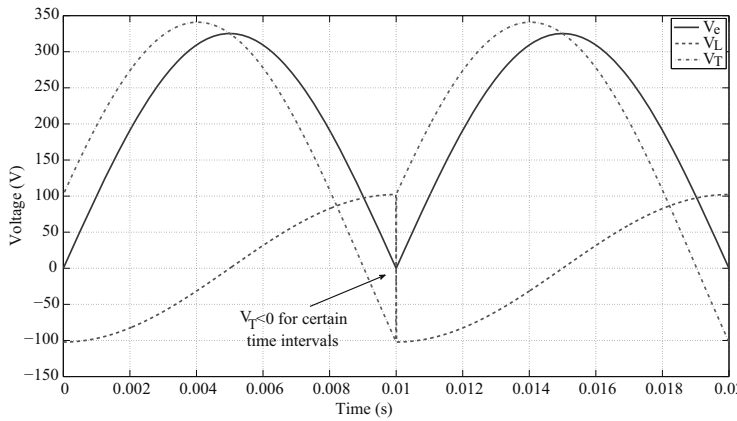


Figure 3.29. *"Low-frequency" waveforms in the PFC transistor. For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

Using these types of converters, we still reach almost unitary power factors, and PFCs are increasingly used in modern computer power supplies; these devices require high-power levels, and often exceed the $600\,\text{W}$ power range where EMC standards for low-frequency conducted disturbances are the least restrictive. An example of a PFC controller is shown

in Figure 3.30: the UC3854 circuit, developed by Unitrode. In this diagram, the controller controls a boost-type converter, powered by a rectifier with an integrated diode (the structure of which is not shown). The control structure is made up of two nested control loops:

– an internal loop to control current i_L in the inductance (measured using a $0.25\,\Omega$ shunt connected to the circuit ground);

– an external loop used to regulate the converter output voltage v_s.

As the objective is for the current to follow a "rectified sinusoid" type profile in phase with the output voltage of the diode rectifier, the output voltage is used to determine a reference value for current i_L.

The boost output voltage is then controlled based on a modulation of the amplitude of the reference value. Qualitatively, it is easy to see that the controller will increase this amplitude if the output voltage is lower than the reference value, and decrease this amplitude in the opposite case.

3.6.4. *Three-phase rectifier without power reversal*

For three-phase rectifiers, we cannot use upstream current regulation form the rectifier to ensure that the input currents are sinusoidal. The reason for this is simple: the conduction intervals of the diodes associated with each phase only cover two-thirds of the network period. We therefore need to place an element downstream from (or at least in parallel to) the rectifier. The simplest solution published to date is known as the Vienna rectifier, or Vienna bridge. This structure was invented (and patented [KOL 93]) in 1993 by Prof. Johann W. Kolar, who taught at the University of Vienna, hence the name. A simplified diagram of the converter is shown in Figure 3.31.

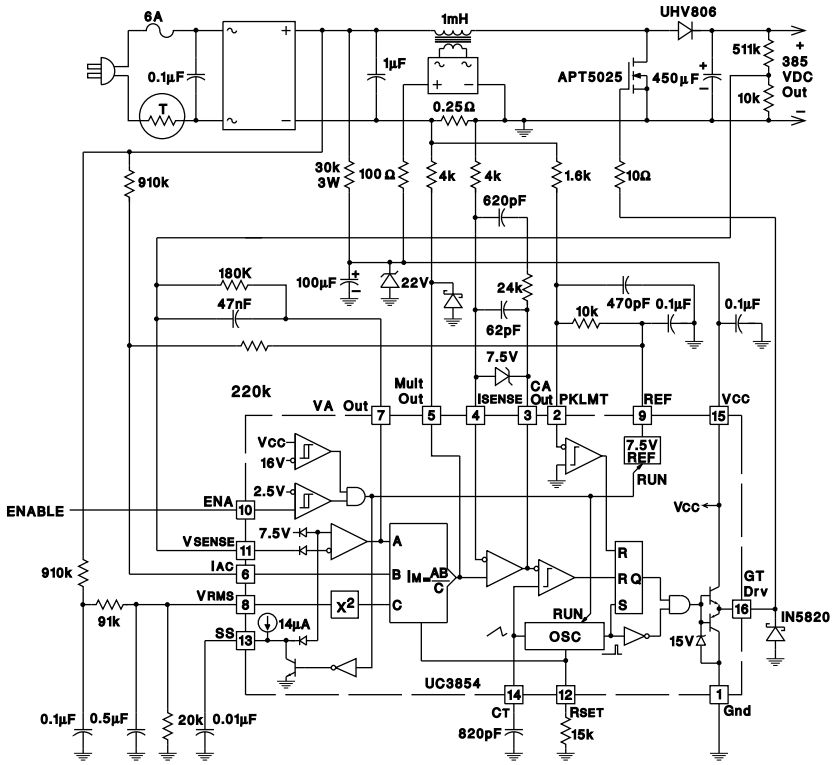


Figure 3.30. *PFC based on a boost converter, controlled by a Unitrode UC3854 circuit*

The switches S_1, S_2 and S_3 used in this structure are four segment switches (voltage- and current-reversible, with controlled switching in both directions). This type of switch was discussed briefly in Volume 1 [PAT 15a], Chapter 2, and will also be discussed in Chapter 4 of the current volume in the context of the PWM dimmer and matrix converters. These switches allow the creation of a kind of active filter, which operates in parallel to a classic diode rectifier, and absorbs not only an active power but also a distorting power. Note that the three switches are interconnected at the mid-point of a capacitor bridge, made up of two capacitors of value C_0 for which the controller needs to ensure voltage balancing.

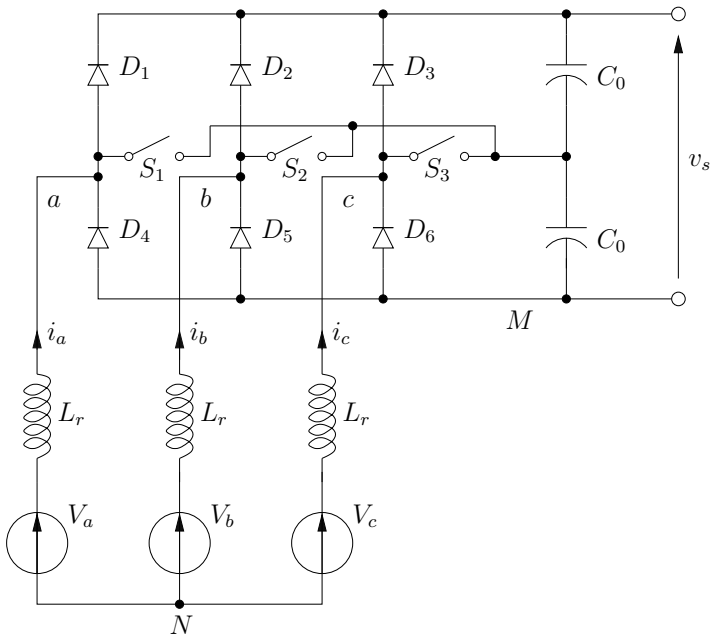


Figure 3.31. *Simplified diagram of a Vienna rectifier*

In analyzing the operation of this converter, a list of possible connection configurations (see Figure 3.32) between the network and the DC bus can be created. Different types of controllers (with fixed or variable frequency) can then be proposed to obtain sinusoidal current input. One "simple" method is to analyze the voltage vectors available as rectifier inputs for each of the presented configurations. This analysis is shown in Table 3.1, which also shows the conditions (for currents) in which the relevant configuration may be obtained. The rectifier output voltage is supposed to be equal to U_0, distributed equally between the two capacitors.

REMARK 3.10.– Note that the transformation used for voltages $v_{\alpha N}$ and $v_{\beta N}$ is the Clarke transform (which preserves amplitudes – see Appendix 1).

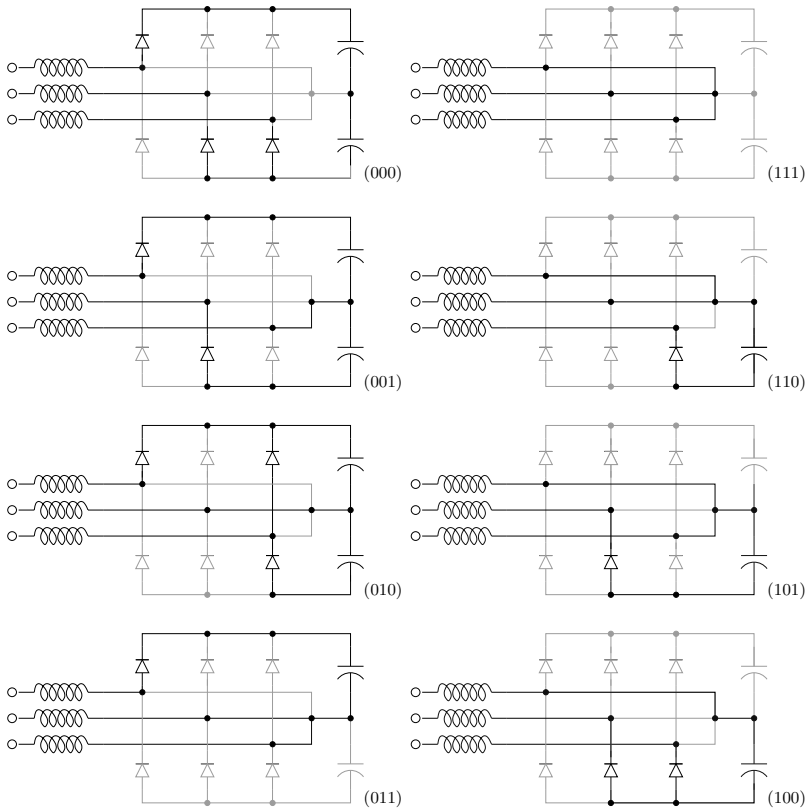


Figure 3.32. *Possible configurations (for 1/6 of a network period) of the Vienna rectifier*

From Table 3.1, the number of accessible levels is important – this converter is similar to multilevel inverters (presented in Chapter 5) – but in this case, the voltage $v_{\alpha N}$ is always positive. This is due to the fact that the presented configurations only represent part of the possible combinations. In fact, there are three possibilities for each half-bridge (upper diode ON or lower diode ON or switch closed). Under these conditions, the full rectifier presents 27 possible configurations: the eight configurations presented above represent only some of the possibilities. An exhaustive

list of the voltage vectors available as input for the rectifier is shown in the two-phase plane $\alpha\beta$ in Figure 3.33. Several of these voltage vectors allow production of a low-frequency PWM-wave synchronous with the network voltage vector, which is able to absorb a sinusoidal current vector without low-frequency distortion (and with HF ripples which can be eliminated easily using a compact EMC filter). The difficulty in the control approach lies in the fact that voltage vectors cannot be obtained unconditionally: the PWM strategy must be limited to those points in the constellation which are genuinely available. Figure 3.33 shows the names of the "(xyz)"-type configurations presented in Table 3.1; most of the rectifier configurations are linked to conditions concerning the sign of the line currents.

Configuration	v_{aN}	v_{bN}	v_{cN}	$v_{\alpha N}/U_0$	$v_{\beta N}/U_0$	*Conditions*
(000)	$2U_0/3$	$-U_0/3$	$-U_0/3$	2/3	0	$i_a > 0, i_b < 0, i_c < 0$
(001)	$-U_0/2$	$-U_0/2$	0	1/2	$-\sqrt{3}/6$	$i_a > 0, i_b < 0$
(010)	$U_0/2$	0	$-U_0/2$	1/2	$\sqrt{3}/6$	$i_a > 0, i_c < 0$
(011)	$U_0/3$	$-U_0/6$	$-U_0/6$	1/3	0	$i_a > 0$
(100)	$U_0/3$	$-U_0/6$	$-U_0/6$	1/3	0	No conditions
(101)	$U_0/6$	$-U_0/3$	$U_0/6$	1/6	$-\sqrt{3}/6$	$i_b < 0$
(110)	$U_0/6$	$U_0/6$	$-U_0/3$	1/6	$\sqrt{3}/6$	$i_c < 0$
(111)	0	0	0	0	0	$i_b < 0, i_c < 0$

Table 3.1. *Partial list of possible configurations of the Vienna rectifier, available input voltage vectors and operating conditions*

For example, configuration (000) is only possible if i_a is positive and i_b and i_c are negative (this is the first configuration presented at the top left of Figure 3.32). In fact, the only configuration shown in the table which does not require specific access conditions is (100). More details concerning this rectifier and applicable control strategies may be found in [VIS 07].

REMARK 3.11.– Another point to consider in designing a control approach for these converters is the need to ensure voltage balancing between the two capacitors (as in the case

of multilevel inverters). For this reason, the current injected by the three switches S_1, S_2 and S_3 at the level of the mid-point connecting the two capacitors must have a strictly null average value.

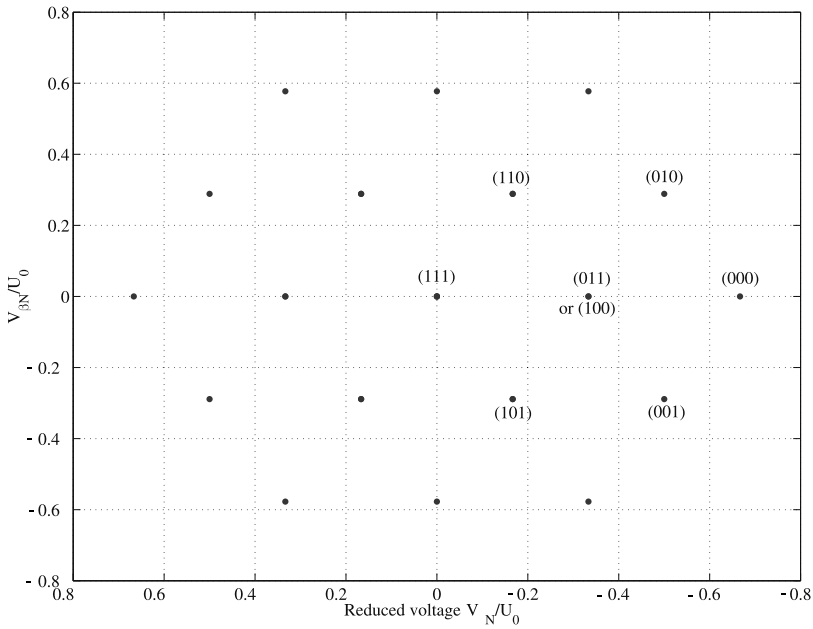


Figure 3.33. *Available input voltage vectors for the Vienna bridge. For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

In conclusion to our study of Vienna rectifiers, Figure 3.34 shows the non-simplified structure of the converter. Switches S_1, S_2 and S_3 are synthesized using three transistors (making the converter easy to control, simply requiring three isolated drivers), "encapsulated" in rectifier bridges to enable voltage and current reversibility. This type of switch will be further considered in the context of matrix converters in the next chapter. However, while this solution offers the advantage of simplicity in control terms, it results in reduced performances in power terms. In the ON state, the voltage drop-off is high,

including both the drop-off associated with the transistor and the drop-offs introduced by the two diodes.

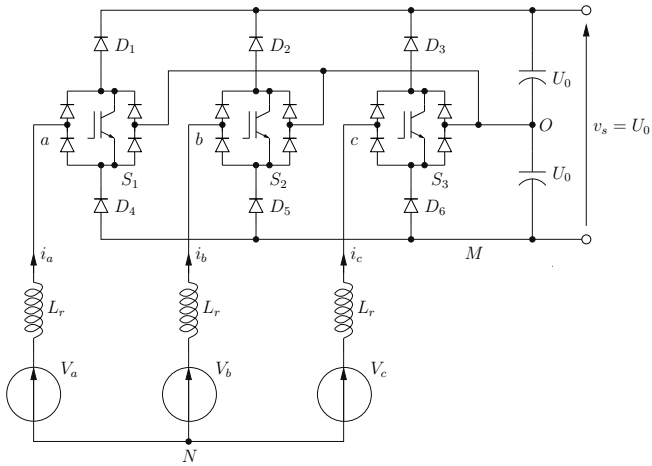


Figure 3.34. *Diagram of a real Vienna bridge*

4

AC/AC Converters

4.1. Two categories

The alternating current/alternating current (AC/AC) family of converters can be split into two distinct groups:

– dimmers, for which the input and output frequencies, respectively, f_1 and f_2, are identical;

– cycloconverters, for which $f_2 \leq f_1$.

Nowadays, we must also consider matrix-based converters; however, these remain relatively scarce due to the complexity of control in comparison to the AC/DC + DC/AC-type structures traditionally used in variable speed drives. This technology, currently undergoing major developments, particularly in aeronautics, will be considered at the end of this chapter.

4.2. Dimmers

4.2.1. *Basic principles*

A dimmer is an AC/AC-type converter with identical input and output frequencies. In this case, the simplest structure consists of placing a four-segment switch, allowing both

voltage and current to be reversible, between a source (generally a voltage source, in the form of the electrical distribution network) and a load. Four-segment switches may be obtained without synthesis (i.e. assembly of components) in the form of a triac. This component, essentially available for low voltages (230 V) and low currents (from a few amperes to tens of amperes at most), is perfectly suitable for use in domestic applications, such as lighting, heating or low-cost variable speed drives for universal motors[1], particularly in portable electrical equipment (e.g. wired electric drills).

Triacs can only be controlled during switch-on (by sending a signal to the trigger), and switch off automatically when the current cancels out. This behavior is close to that of the thyristor (except in terms of voltage and current reversibility). For high-power applications, it is possible to replace a triac by two thyristors, placed top-to-tail. These converters are used to start asynchronous motors in industrial environments (in this case, the converters act as starting components, and not as variable speed drives) and in installations for dynamic compensation of reactive power (static synchronous compensator (STATCOM)). The latter application will be discussed in a separate section below.

4.2.2. *Single-phase dimmer*

4.2.2.1. *Structure*

The simplest structure for a single-phase dimmer is based on a triac. The power structure of this converter is very simple, as shown in Figure 4.1 (with a resistive load, in this case).

1 Universal motors are direct current (DC) motors with series excitation, which develop a torque proportional to the square of the current. They are, therefore, not sensitive to current reversal, and are thus entirely suitable for use with AC current power supplies.

Triacs are bidirectional in terms of both voltage and current, with controlled switch-on and spontaneous switch-off when the current through the component cancels out. This means that these components are controlled (via the trigger) by generating control pulses synchronous with the input voltage $v_e(t) = V_{e\max}.\sin(\omega t)$ for each half-period. If we consider an angle varying between 0 and 2π for a period, it is possible to identify the instants at which control pulses are triggered by a unique angle ψ such that pulses occur at instants corresponding to the angles ψ and $\pi + \psi$.

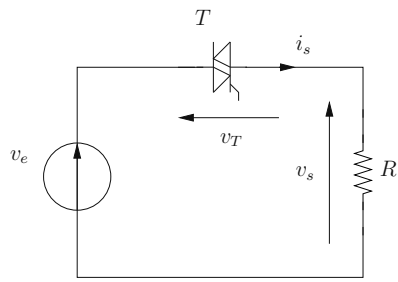


Figure 4.1. *Single-phase triac dimmer*

4.2.2.2. *Case of resistive load*

Over a resistive load (staying with the diagram in Figure 4.1), we see that:

$$i_s = \frac{v_s}{R} \qquad [4.1]$$

and only two modes of operation are possible:

– if T is OFF, we have $i_s = 0$ and thus $v_s = 0$;

– if T is ON, we have $v_T = 0$; hence $v_s = v_e = V_{e\max}.\sin(\omega t)$ and thus $i_s = \frac{V_{e\max}}{R} \cdot \sin(\omega t)$.

The waveforms corresponding to an angle $\psi = 30°$ are shown in Figure 4.2. Theoretically speaking, the control angle ψ may vary between 0 and 180°; in practice, however,

limitations are often imposed either by the control mechanism or by the triac itself. If the current circulating in the component in the ON state is not sufficient (notably, when voltage v_e is close to 0), the triac switches off immediately after the end of the control pulse train.

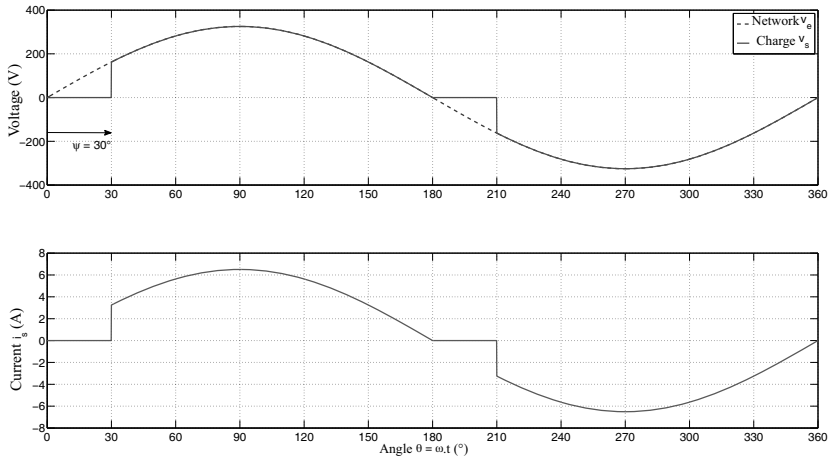


Figure 4.2. *Voltage/output current waveforms for a single-phase triac dimmer over a resistive load*

From this simple case, we may calculate the active, reactive and apparent powers and the power factor, and even $\cos\varphi_1$ (considering the fundamental component of the absorbed current alone). It is also possible to evaluate the harmonic distortion rate of the voltage and current supplied to the load.

First, note that the RMS voltage provided by the network is equal to $\frac{V_{e\max}}{\sqrt{2}}$. If we wish to calculate the RMS value $I_{s\mathrm{RMS}}$ of the current i_s (both as input and output from the converter), the following general definition is required:

$$I_{s\mathrm{RMS}} = I_{e\mathrm{RMS}} = \sqrt{\frac{1}{T}\int_{\frac{\psi T}{2\pi}}^{T}\left(\frac{V_{e\max}}{R}\right)^2 \sin^2(\omega t)\,.dt} \qquad [4.2]$$

After changing the variable (and following integration for a half-period), we obtain the following result:

$$I_{s\mathrm{RMS}} = \frac{V_{e\max}}{R}\sqrt{\frac{1}{2\pi}\int_{\psi}^{\pi}\left(1-\cos\left(2\theta\right)\right).d\theta} \qquad [4.3]$$

$$I_{s\mathrm{RMS}} = \frac{V_{e\max}}{R}\sqrt{\frac{1}{2\pi}\left(\pi-\psi+\frac{\sin\left(2\psi\right)}{2}\right)} \qquad [4.4]$$

Using this result, we can give an expression of the active power entering and exiting the converter, which is presumed to be ideal ($P_e = P_s$):

$$P_e = P_s = R.I_{s\mathrm{RMS}}^2 = \frac{V_{e\max}^2}{R}\left[\frac{1}{2\pi}\left(\pi-\psi+\frac{\sin\left(2\psi\right)}{2}\right)\right] \qquad [4.5]$$

We can also calculate the apparent input power S_e:

$$S_e = \frac{V_{e\max}}{\sqrt{2}}I_{e\mathrm{RMS}} = \frac{V_{e\max}^2}{\sqrt{2}R}\sqrt{\frac{1}{2\pi}\left(\pi-\psi+\frac{\sin\left(2\psi\right)}{2}\right)} \qquad [4.6]$$

From this, we deduce the expression of the input power factor Fp_e:

$$\mathrm{Fp}_e = \frac{P_e}{S_e} = \sqrt{\frac{1}{\pi}\left(\pi-\psi+\frac{\sin\left(2\psi\right)}{2}\right)} \qquad [4.7]$$

We can easily verify the operating point at $\psi = 0°$ for which the load R is constantly connected to the network. Thus, we obtain:

$$\begin{cases} I_{s\mathrm{RMS}} = I_{e\mathrm{RMS}} = \frac{V_{e\max}}{R\sqrt{2}} \\ P_e = P_s = \frac{V_{e\max}}{2R} \\ S_e = P_e = \frac{V_{e\max}}{2R} \\ \mathrm{Fp}_e = 1 \end{cases} \qquad [4.8]$$

We may also consider the fundamental component $i_{e1}(t)$ of the current absorbed as input into the converter, with the expression:

$$i_{e1}(t) = I_d.\sin(\omega t) + I_q.\cos(\omega t) \qquad [4.9]$$

where:

$$I_d = \frac{2}{T}\int_0^T i_{e1}(t).\sin(\omega t).dt \qquad [4.10]$$

and:

$$I_q = \frac{2}{T}\int_0^T i_{e1}(t).\cos(\omega t).dt \qquad [4.11]$$

It then becomes possible to calculate the two components I_d and I_q after a classic change of variable ($\theta = \omega t$):

$$\begin{cases} I_d = \frac{2}{\pi}\int_\psi^\pi \frac{V_{emax}}{R}\sin^2\theta.d\theta \\ I_q = \frac{2}{\pi}\int_\psi^\pi \frac{V_{emax}}{R}\sin\theta.\cos\theta.d\theta \end{cases} \qquad [4.12]$$

As before, we may use classic trigonometric formulas to transform the functions under the $\int$ sign:

$$\begin{cases} \sin^2\theta = \frac{1}{2}(1-\cos(2\theta)) \\ \sin\theta.\cos\theta = \frac{1}{2}\sin(2\theta) \end{cases} \qquad [4.13]$$

hence:

$$\begin{cases} I_d = \frac{V_{emax}}{\pi R}\int_\psi^{2\pi}(1-\cos(2\theta)).d\theta = \frac{V_{emax}}{\pi R}\left(\pi - \psi + \frac{1}{2}\sin(2\psi)\right) \\ I_q = \frac{V_{emax}}{\pi R}\int_\psi^{2\pi}\sin(2\theta).d\theta = \frac{V_{emax}}{\pi R}(1-\cos(2\psi)) \end{cases} \qquad [4.14]$$

These results are illustrated in Figure 4.3. Giving closer consideration to the trace of location $(I_q(\psi), I_d(\psi))$, we see that

component I_q is placed on the X axis and I_d on the Y axis; the phase reference is the Y axis, as the power voltage supplied to the dimmer is in "sine" form. Note that the "current" vector presents a systematic lag in relation to the "voltage" vector (with the exception of the specific cases where $\psi = 0°$ and $\psi = 180°$). Clearly, in the context of the approximation to the 1^{st} harmonic (i.e. the fundamental), the dimmer, associated with a resistive load, behaves in the same way as an inductive load consuming a reactive power $Q > 0$.

4.2.2.3. *Case of inductive loads*

The layout of the structure using a purely inductive load L remains identical to that shown in 4.1. However, the relationship between the output voltage v_s and the current $i_e = i_s$ is no longer $v_s = R.i_s$, but rather:

$$i_s = \frac{1}{L} \int v_s\,(t)\,.dt \qquad [4.15]$$

To ensure correct control of this element, we begin by considering that the control angle ψ takes the form $\frac{\pi}{2} + \widetilde{\psi} + k\pi$ (where $\widetilde{\psi} \geq 0$ and $k \in \mathbb{Z}$).

In the case where $\psi = \frac{\pi}{2} + k\pi$, we see that the current only cancels out at instants, corresponding to $\theta = \omega.t = \frac{\pi}{2} + k\pi$, and not over time intervals, giving a permanent connection of inductance L to the network. When $\widetilde{\psi}$ is non-null, the operating mode includes non-intermittent current canceling phases. To study the behavior of the converter in this case, we begin by noting the expression of $v_e(t) = V_{\text{emax}}.\sin(\theta)$, which is then integrated to calculate i_s in accordance with [4.15]:

$$i_s\,(\theta) = \frac{V_{\text{emax}}}{L\omega} \int_{\frac{\pi}{2}+\widetilde{\psi}}^{\theta} \sin(\xi).d\xi = \frac{V_{\text{emax}}}{L\omega} \left[-\cos\xi\right]_{\frac{\pi}{2}+\widetilde{\psi}}^{\theta} \qquad [4.16]$$

This gives us:

$$i_s\,(\theta) = \frac{V_{\text{emax}}}{L\omega} \left(\cos\left(\frac{\pi}{2} + \widetilde{\psi}\right) - \cos\theta\right) \qquad [4.17]$$

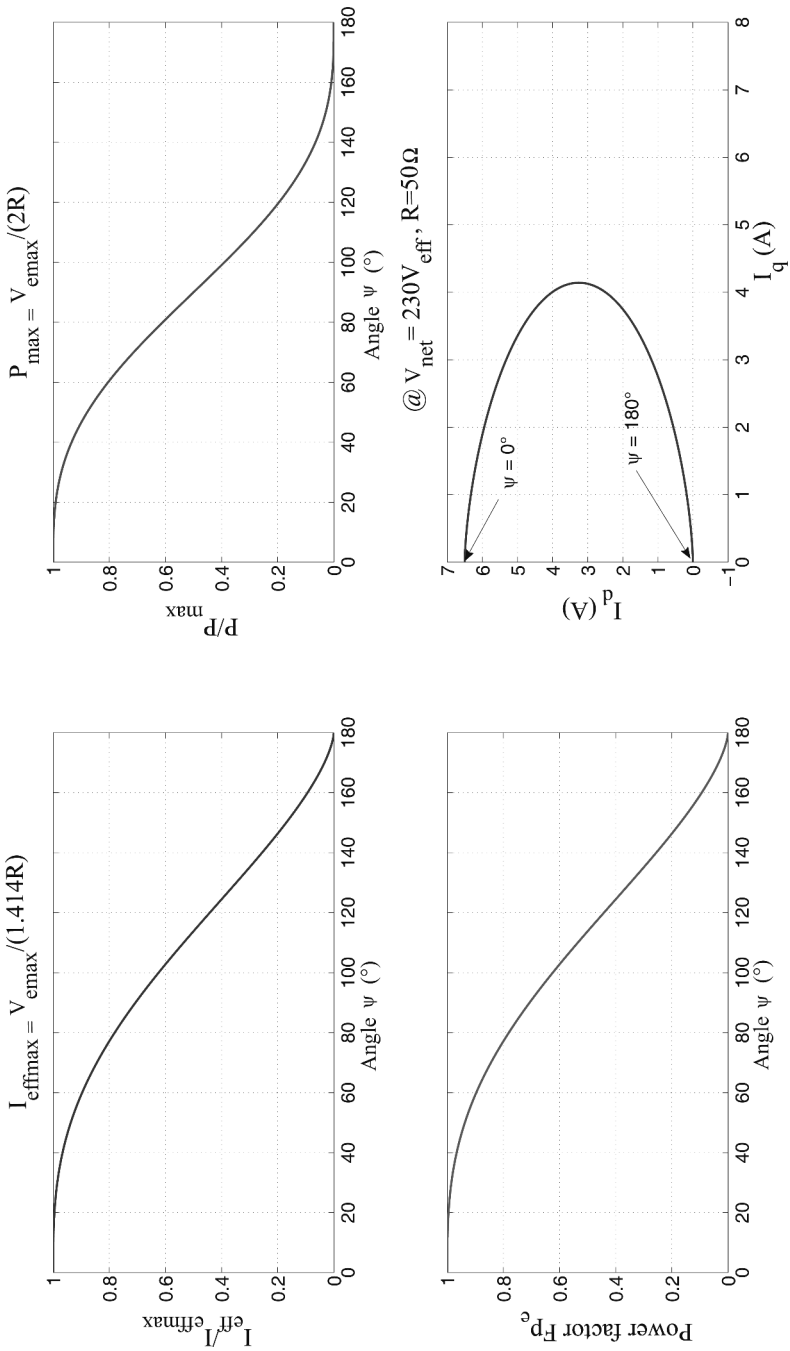


Figure 4.3. *Summary of operating characteristics of a single-phase triac dimmer*

The triac is, therefore, in a state of conduction over an angular interval from $\theta_1 = \frac{\pi}{2} + \widetilde{\psi}$ to $\theta_2 = \frac{3\pi}{2} - \widetilde{\psi}$. For the negative alternation, the triac effectively enters into conduction over the interval $\left[\frac{3\pi}{2} + \widetilde{\psi}; \frac{5\pi}{2} + \widetilde{\psi}\right]$. An example of waveforms is shown in Figure 4.4 for $\psi = 120°$ (for $V_{\text{emax}} = 230\,\text{V}$; $f = 50\,\text{Hz}$; $L = 100\,\text{mH}$).

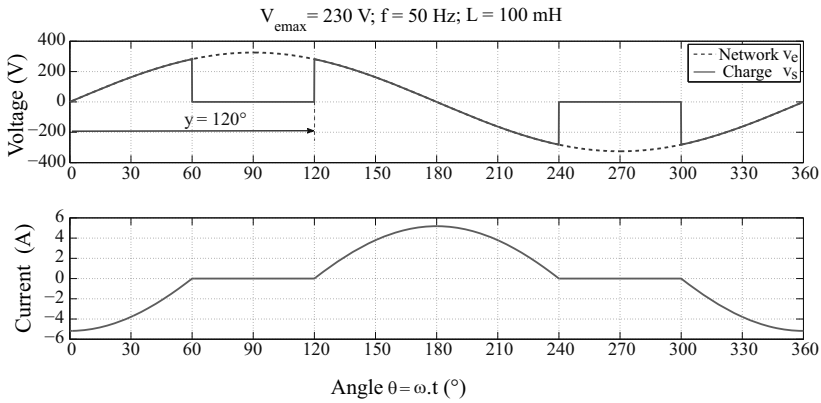


Figure 4.4. *Example of operation of a single-phase triac dimmer using an inductive load*

4.2.2.4. *Dissymmetry in triacs*

Triacs present a drawback which can be problematic when using inductive loads of the "transformer + secondary load" type, in the form of dissymmetric behavior with low load currents. These components require a minimum current in order to switch on effectively after the gate has received a pulse: if the minimum current is not reached, the triac opens spontaneously immediately after the end of the control pulse. This is only really problematic due to the difference in the minimum current threshold for positive and negative half-waves. In practice, a triac may allow a low current to pass in one half-wave (for example, positive), but remains closed for the other half-wave under the same operating conditions. In cases involving powering the primary of a transformer, this behavior is problematic as it leads to the

application of a non-null average voltage; this causes a modification in the average state of the magnetic core, which rapidly leads to saturation. In this situation, the value of the magnetizing inductance of the transformer falls, leading to a very high current draw. This almost systematically leads to the destruction of either the triac or the fuse used to protect the component: in both cases, the converter will fail.

One solution to this problem consists of using a thyristor, placed in the "continuous" diagonal of a Graetz bridge (see Figure 4.5). The single thyristor is always used in the same way for both directions of current circulation, and no dissymmetry is present in this configuration.

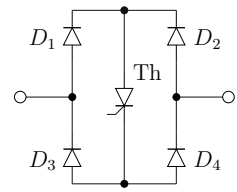


Figure 4.5. *Triac alternative using a thyristor*

REMARK 4.1.– It is also possible to use two thyristors, placed head-to-tail, notably in cases with high power levels. However, this solution poses the same problem as the triac. Dispersion may occur from one component to another (with the same reference) for the value of the minimum current needed to maintain conduction.

4.2.3. *Three-phase situation*

Three-phase dimmers are used in soft starters for induction machines. These devices limit the current draw from the network during starting, and limit torque ripples in the mechanical load of the machine. This starting technique allows a more progressive increase in the power supply voltage than in "star–delta" starters, or than obtained by

removing statoric resistors (or rotoric resistors in the case of wound rotor machines). These components are based on antiparallel associations of thyristors, essentially due to the power values involved (normally higher than those encountered with triac dimmers). A variety of assemblies are possible, using star or delta connections. The subject of three-phase converters is relatively complex due to phase coupling. Note, however, that in certain conditions, we encounter a situation equivalent to that found using three independent single-phase dimmers. The readers may wish to consult [ROM 86], which is devoted to AC/AC conversion with a focus on dimmers.

4.2.4. *STATCOM*

One application of dimmers is in the static compensation of reactive power. This is achieved using STATCOM, in contrast with electromechanical compensators, i.e. synchronous machines. Our aim is to reduce the reactive power drawn from the network; as we will see, the dimmer allows us to implement rapid changes in the reactive power. The same effect is achieved in wound-inductor synchronous machines by controlling the excitation current.

An electrical installation classically consumes a certain reactive power (generally positive, due to the inductive behavior of many loads, such as electrical machines and transformers). This power has an undesirable effect on the dimensioning of all equipment located upstream within the network (transformers, cables, general equipment, alternators, etc.). The dimensioning of these elements is based on the apparent power S of the installation and not on the active power P which is actually consumed: the reactive power Q is involved due to the following relationship (only valid in sinusoidal mode):

$$S^2 = P^2 + Q^2 \qquad [4.18]$$

Given the inductive character of the installation, it is logical to place capacitors at the entry point in order to compensate the consumed reactive power. We can then cancel out the reactive power drawn from the network, allowing us to optimize the system. In practice, we generally do not aim to cancel out the reactive power, but to limit it to an acceptable level ($\cos\varphi = 0.93$ or $\tan\varphi = 0.5$). This objective may be hindered by a major issue: power consumption may fluctuate, and in this case, the permanent inclusion of capacitors does not solve the problem, and may even generate new issues.

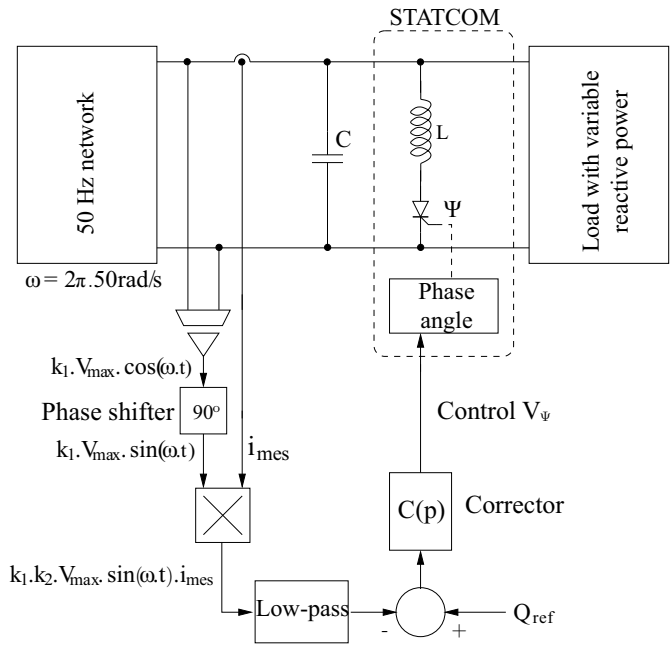
In this case, we need to analyze the behavior of the installation in terms of the speed of fluctuation in consumption. In the case of slow fluctuations (on a scale of several hours), we may adjust the use of capacitors, connecting or disconnecting them from the network as required. This is known as a capacitor bank installation. Unfortunately, this solution is not suitable for rapid fluctuations[2] (from approximately 1 min to 1 s) which may be encountered in certain industrial applications (such as arc furnaces). This is the context of application of STATCOMs. Section 4.2.2 has already dealt with the behavior of a single-phase dimmer connected to an inductance; this device may be used to modulate consumption of reactive energy between a maximum value $Q_{L\max} = \frac{V_{e\max}^2}{L\omega}$ and 0 by simply adjusting the control angle ψ of the dimmer within the range between 90 and 180°. This means of controlling reactive power is very fast (of the order of $20\,\text{ms}$ for a $50\,\text{Hz}$ network). Therefore, we need to characterize the electrical installation in which the STATCOM is to be implemented, in terms of the minimum $Q_{\min}$ and maximum $Q_{\max}$ acceptable consumption of reactive power, before carrying out the following dimensioning process:

2 The connection of capacitors in a high-power network creates strong current draws, which are particularly stressful for the switches involved. This means that they cannot be switched too often.

– choice of a capacitor (or group of capacitors) C able to compensate $Q_{\max}$ (i.e. $Q_{\max} = C\omega V_{e\max}^2$);

– choice of an inductance L able to consume the excess reactive power supplied by the capacitor when the network is only consuming $Q_{\min}$ (i.e. $Q_{\max} - Q_{\min} = \frac{V_{e\max}^2}{L\omega}$).

Thus, STATCOM implementation requires a measurement of the reactive power upstream of the installation (STATCOM, capacitors and the load "consuming" variable reactive power), alongside regulation of this reactive power to a null reference value Q_{ref} (or at least to a value which respects the constraints imposed by the distribution contract). An overview of the structure of this system is shown in Figure 4.6.



Remark: switching frequency well below 100 Hz

Figure 4.6. *Overview of the STATCOM and control systems*

REMARK 4.2.– It is important to note that the operating mode of the dimmer is not sinusoidal (except for the operating point where $\psi = 90°$). This means that a harmonic filtering issue remains after the installation of the STATCOM. This may be resolved by the use of antiharmonic filters for the most important components. For this, we simply associate the capacitor C (split into several components, C_k) with series inductances L_{sk}, which allow us to fix pulsation resonances $\omega_k = \frac{1}{\sqrt{L_{sk}C_k}}$; these constitute low-impedance traps for the corresponding harmonic currents.

4.2.5. *PWM dimmers*

The main problem associated with the use of triac- or thyristor-based dimmers, as seen above, is the impossibility of controlled switch-off; this means that the switching frequency is imposed by the frequency of the "network" voltage. As this frequency is low, the generated harmonics are close to the fundamental (useful) frequency, making the filtering difficult. From an application perspective, this may be negligible due to high inertia (for example, for lighting or furnace power supplies); from a network perspective, however, harmonics may lead to disturbances (conductions) which are incompatible with electro magnetic compatibility (EMC) standards. Transistor-based pulse-width modulation (PWM) dimmers may be particularly interesting from this perspective, as they permit high frequency (HF) switching (from approximately 10 to 100 kHz); this makes filtering considerably easier (with a consequent, and considerable, reduction in the size of components required). Having said that, single-phase PWM dimmers are considerably more complex than their triac equivalents, as shown in Figure 4.7.

If we apply a sinusoidal input voltage $v_e(t) = V_{\text{emax}}.\sin(\omega t)$ and we control switch pairings (K_1, K_4) and (K_2, K_3) in a complementary manner, as in the case of a four-quadrant chopper, we obtain a voltage waveform v_s of the type

presented in Figure 4.8. This result was obtained for a $230\,\mathrm{V_{RMS}}$, $50\,\mathrm{Hz}$ network (frequency denoted as F_{net}) with a switching frequency F_d of $1\,\mathrm{kHz}$ (a low value was selected for this frequency to allow visualization of the division).

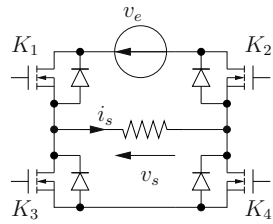


Figure 4.7. *PWM dimmer with MOSFET transistors*

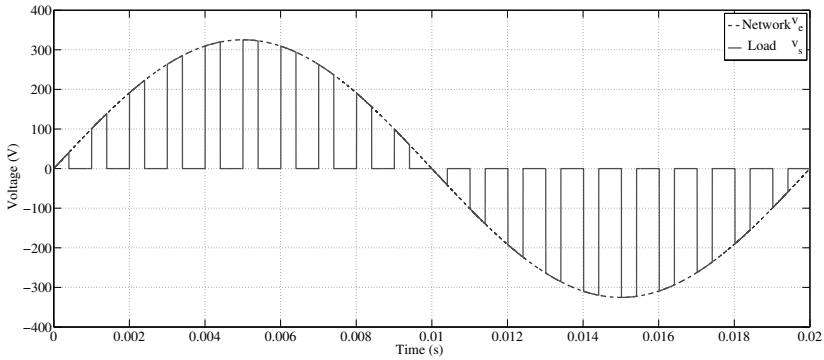


Figure 4.8. *Waveform of the voltage output of a PWM dimmer*

Using this type of control, we see that the amplitude $V_{s1\max}$ of the fundamental component of the voltage v_s is piloted in a linear manner, as a function of the duty ratio α of the bridge control and the effective "network" voltage $V_{e\max}$:

$$V_{s1\max} = \alpha.V_{e\max} \qquad [4.19]$$

Harmonic components are rejected around the switching frequency F_d (at F_d, $F_d + F_{\mathrm{net}}$, $F_d - F_{\mathrm{net}}$, ...) and its multiples.

REMARK 4.3.– The diagram in Figure 4.7 shows a purely resistive load. In practice, this is never the case (any resistive

load is also potentially inductive, due to the connections or the resistor technology involved). This can be problematic, as, in classic converters using voltage switches (transistors), as seen above, transistor switch-off is associated with spontaneous diode conduction. However, using this new converter technology, the free wheel phenomenon is no longer possible; a current source circuit may, therefore, be open, which is potentially destructive for components (due to overvoltage). This problem will be discussed in section 4.5.3 in the context of the broader family of matrix converters, which includes PWM dimmers.

4.3. Choice between PWM, phase angles and wave trains

As we have seen, it is possible to create phase angle-controlled dimmers using triacs or thyristors, which allow us to control the output voltage of a converter at the level of a network period (or, more precisely, a half-period, i.e. 10 ms for a network at 50 Hz). It is also possible to synthesize a dimmer using transistors; in this case, the switching frequency becomes much higher (easily reaching tens of kHz for average power levels – i.e. the order of one kilowatt). A further solution which has not yet been discussed in this chapter, but which was mentioned in Chapter 1 of Volume 1 [PAT 15a], is operation using wave trains. This technique (which is similar to chopping) consists of allowing M periods of the network voltage to pass over a full wave train of N periods. It is immediately evident that the response time of this type of control is much longer than for the other two options, and in this case, we may envisage the use of a different type of switch: electromechanical networks can be used if the switching frequency is sufficiently low. However, as the ability to switch at zero voltage is desirable (due to the generation of disturbances), electronic switches are still

preferred (static relay[3] – see Figure 4.9). Switching must be sufficiently controlled in terms of switch reactivity.

Figure 4.9. *Static relay*

As an example, if we wish to obtain a fine-tuning resolution of approximately 1%, we should choose a wave train at $N = 100$, giving a control periodicity of $2\,\mathrm{s}$ for a $50\,\mathrm{Hz}$ network. In these conditions, switching remains fairly rapid, and a mechanical switch would not be ideal. Moreover, we need to guarantee switching for whole voltage periods in order to avoid average current consumption in the network.

Based on these considerations, we see that control response time is a key criterion for use in choosing between different dimmer control techniques (which also impact the components used in the power structure). This response time should be adapted to suit the load response time:

– for a required response time of approximately 1 s (or more), the wave train approach is entirely suitable;

– for a response time of around one-tenth of a millisecond, phase angle control is most suitable;

– for response times of under one-tenth of a millisecond, PWM control becomes necessary.

3 Using an AC current, this is often a photo-triac (with a galvanically isolated control).

Evidently, PWM control may be used in all these cases, but (for reasons of complexity) its cost is considerably higher than that involved using static relays and wave train control, or in phase angle-controlled dimmers.

4.4. Cycloconverters

Another type of AC/AC converter which we have not yet considered is the cycloconverter. As shown in section 4.1, this type of converter allows us to pass directly from an alternating network to an alternating load using a different frequency without needing to pass through an intermediary DC bus (see Figure 4.10), which is not the case when using a classic variable speed drive.

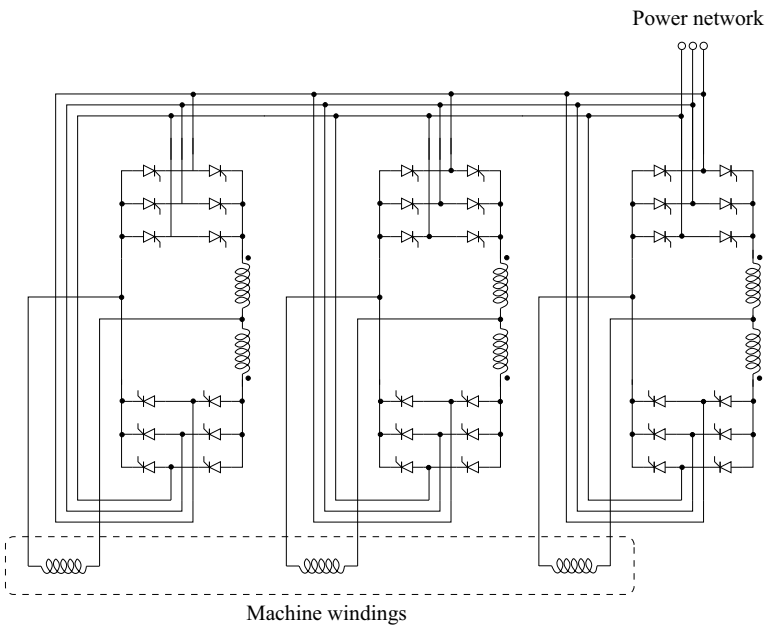


Figure 4.10. *Three-phase cycloconverter*

Cycloconverters for use with three-phase machines may be seen as three antiparallel associations of PD3 thyristor

rectifiers, as shown in Figure 3.23. These three associations are used to power the three windings of a three-phase machine, with one constraint: it is not possible to power the machine with a frequency higher than that of a network. We simply need to modulate the control angle ψ of the three associations to produce a balanced three-phase power supply (direct or inverse). Note, however, that this type of converter is used increasingly rarely due to the progress made in power electronics concerning other categories of components (notably, IGBTs) and the limitations of this specific structure.

REMARK 4.4.– As we have seen, the structure of a single-phase inverter is the same as that of a four-quadrant chopper, but with a control which is no longer constant, but takes place at a low frequency (in comparison with the switching frequency). The same is true for the cycloconverter: the association of two antiparallel thyristor rectifiers constitutes a four-quadrant AC-DC converter which may be used in variable mode. Note, however, that the switching frequency used for this type of converter is very low; consequently, the fundamental frequency is limited, and the ratio between the two frequencies is low. This, therefore, produces a power supply of limited quality (see the real waveform V_{OF} shown in Figure 4.11, for a reference value denoted as V_O). For this reason, this type of converter is only used for very specific application types (high power levels and low dynamic performance), as practically the only advantage of the component lies in its low cost.

4.5. Matrix converters

4.5.1. *Basic structure*

Direct AC-AC conversion may be carried out using PWM dimmers to regulate the amplitude of the voltage supplied to the load without modifying the frequency. It is also possible to carry out “cycloconverter”-type conversions using matrix

converters. This technique involves the use of transistor switches and diodes, operating at high frequencies and offering far better performances than those offered by converters such as those presented in Figure 3.24. Recent developments concerning this converter type, notably in aeronautics, suggest a bright future for the component. Its main interest lies in offering an alternative to the classic indirect solution used for variable speed drives, as shown in Figure 1.1 of Chapter 1 of Volume 1 [PAT 15a], i.e. the association of a rectifier and an inverter. In this structure, the LC filter, and more precisely the electrolytic capacitor used for voltage smoothing, is seen as an unacceptably weak point for equipment where a high level of reliability is needed. As we will see, matrix converters allow us to connect two alternating sources directly, without the use of passive intermediary elements. This offers gains not only in terms of reliability, but also in terms of volume and weight in electronic power converters: these parameters are also fundamental criteria in dimensioning onboard equipment generally, and particularly in the aeronautics industry.

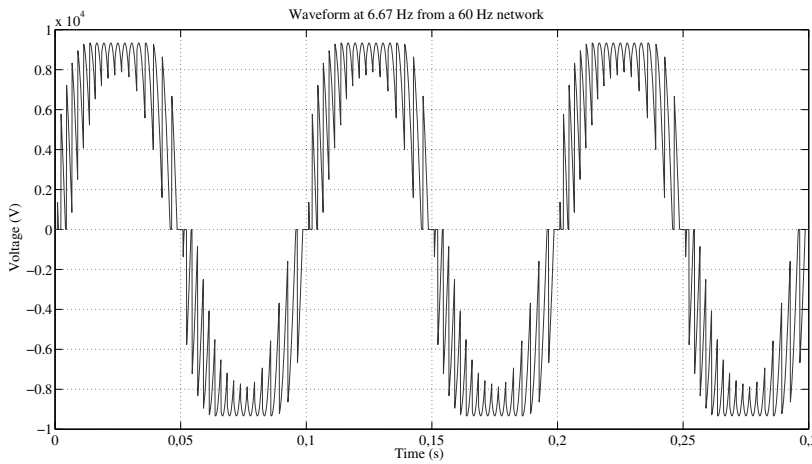


Figure 4.11. *Waveform of the output voltage of a cycloconverter*

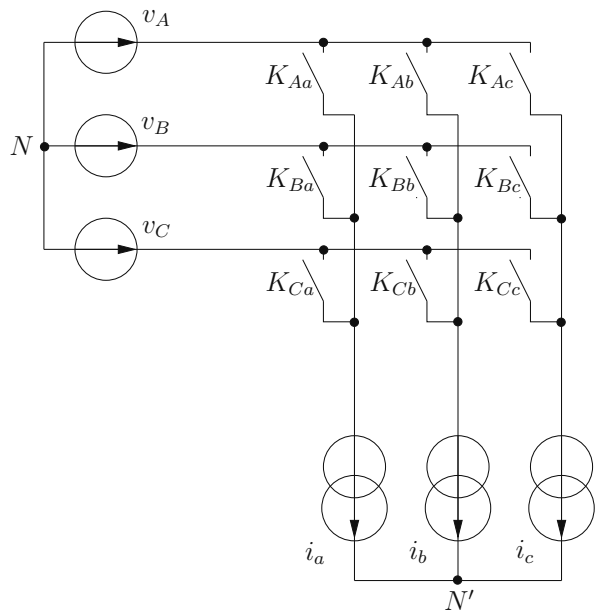


Figure 4.12. 3×3 *matrix converter*

The converter shown in Figure 4.12 connects three voltage sources (three-phase network) to three current-source-type loads (three-phase electrical machine). To do this, we use a grid made up of nine switches (3×3). This type of converter (and this topology) can easily be generalized to connect a source using m phases to a load using n phases via a grid made up of $m \times n$ switches.

The switches used in this type of converter must be reversible in terms of both voltage and current. We, therefore, use a synthesized switch similar to that shown in Chapter 2 of Volume 1 [PAT 15a], Figure 2.16. In practice, this switch is modified to make it easier and less costly to use. Two equivalent solutions (based on IGBT) are shown in Figure 4.13. In both cases, the intermediary points between the transistor and the diode on both branches are connected, which was not the case in the switch proposed in Volume 1:

this changes nothing from a user perspective. Note that in configuration “b”, the emitters of the two transistors are connected to a common potential. This means that the two transistors may be controlled using drivers powered by a common floating source, simplifying close control and thus reducing the overall cost of the converter, as this applies to all of the switches in the converter (nine switches, in our specific case).

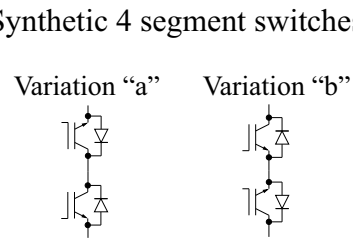


Figure 4.13. *Synthesized four-segment switches (two variations)*

Another type of four-segment switch exists, similar to that proposed as a replacement for a triac in Figure 4.5; however, this switch (see Figure 4.14) introduces a voltage drop-off corresponding to three components, rather than two, as in the case of the synthesized switches shown in Figure 4.13.

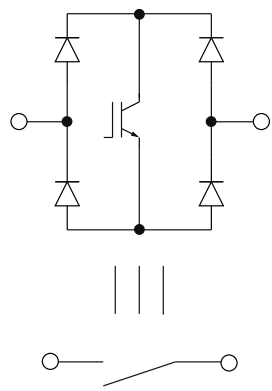


Figure 4.14. *Synthesized four-segment switch with a single IGBT*

4.5.2. *Operating principle*

Let us presume that this converter is powered by an ideal network with a phase voltage of $230\,\mathrm{V}$ at $50\,\mathrm{Hz}$. The variation band for the converter output voltage can be easily identified based on the waveforms in Figure 4.15: for each instant, we must simply identify the values of $\max(v_a, v_b, v_c)$ and $\min(v_a, v_b, v_c)$.

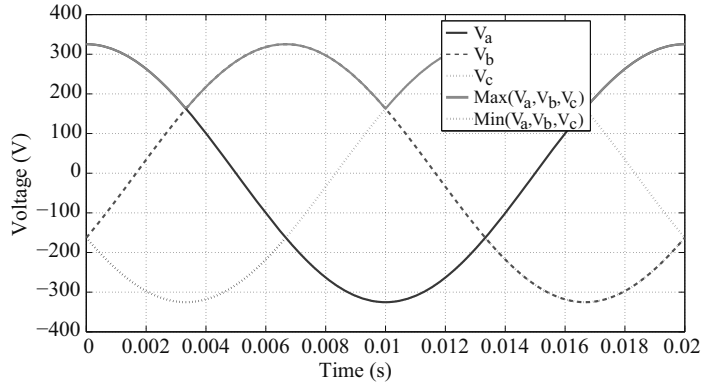


Figure 4.15. *Three-phase (simple) voltage system Veff* = $230\,V$, *f* = $50\,Hz$. *For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

The system of output voltages may be described in matrix form as a function of the system of input voltages and the state of the switches, as in the case of inverters, in order to design a satisfactory control strategy for this type of converter. Each switch K_{Xy} is associated with a switching function f_{Xy} ($X \in A, B, C$ and $y \in a, b, c$) with values of 0 or 1 corresponding to an open or closed state. The converter input current vector i_X may be equated as a function of the output current vector i_y and the switching function matrix. This equation system is easy to generalize, but in this specific case (3×3), we have:

$$\begin{pmatrix} i_A \\ i_B \\ i_C \end{pmatrix} = \begin{pmatrix} f_{Aa} & f_{Ab} & f_{Ac} \\ f_{Ba} & f_{Bb} & f_{Bc} \\ f_{Ca} & f_{Cb} & f_{Cc} \end{pmatrix} \cdot \begin{pmatrix} i_a \\ i_b \\ i_c \end{pmatrix} \qquad [4.20]$$

The source interconnection rules allow us to close several switches from the same line; however, we may not close two switches from the same column, as this would lead to a short-circuit in several voltage sources. On the other hand, all of the switches in the same column should not be left open, as this leaves a current source in an open circuit. To summarize, one single switch should be closed in each column, and each column may be controlled independently of the others.

On this basis, we see that at each instant the voltages v_{yN} are defined with a value of v_a, v_b or v_c. In a general manner, it is thus possible to write:

$$\begin{cases} v_{aN} = f_{Aa}.v_a + f_{Ba}.v_b + f_{Ca}.v_c \\ v_{bN} = f_{Ab}.v_a + f_{Bb}.v_b + f_{Cb}.v_c \\ v_{cN} = f_{Ac}.v_a + f_{Bc}.v_b + f_{Cc}.v_c \end{cases} \quad [4.21]$$

There is no risk of error, as for each line only one connection function f_{Xy} has a value of 1 (one function must always have this value).

In matrix form, we obtain:

$$\begin{pmatrix} v_{aN} \\ v_{bN} \\ v_{cN} \end{pmatrix} = \begin{pmatrix} f_{Aa} & f_{Ba} & f_{Ca} \\ f_{Ab} & f_{Bb} & f_{Cb} \\ f_{Ac} & f_{Bc} & f_{Cc} \end{pmatrix} \cdot \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \quad [4.22]$$

As for inverters, to characterize the power supply to a load (as output), we do not consider voltages referenced in relation to the neutral of the power supply (input) but in relation to the neutral of the load, denoted by N' in Figure 4.12, which we presume to be connected using a star connection. If we consider that the load is balanced and has a passive R-L impedance (and not made up of ideal current sources), we may apply Millmann's theorem to calculate the potential

$v_{N'N}$ of the neutral N' of the load in relation to the neutral N of the input source:

$$v_{N'N} = \frac{v_{aN} + v_{bN} + v_{cN}}{3} \qquad [4.23]$$

The difficulty in this case, compared to the inverter, lies in the fact that these values are not constant. The voltages encountered by the load are thus written (for $x \in a, b, c$):

$$v_{xN'} = v_{xN} - v_{N'N} \qquad [4.24]$$

In matrix form, this gives:

$$\begin{pmatrix} v_{aN'} \\ v_{bN'} \\ v_{cN'} \end{pmatrix} = \left[\mathbb{I}_3 - \frac{1}{3} \begin{pmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{pmatrix} \right] . \begin{pmatrix} f_{Aa} & f_{Ba} & f_{Ca} \\ f_{Ab} & f_{Bb} & f_{Cb} \\ f_{Ac} & f_{Bc} & f_{Cc} \end{pmatrix} . \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \qquad [4.25]$$

This corresponds to the classic matrix:

$$\begin{pmatrix} v_{aN'} \\ v_{bN'} \\ v_{cN'} \end{pmatrix} = \underbrace{\frac{1}{3} \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix}}_{G} . \begin{pmatrix} f_{Aa} & f_{Ba} & f_{Ca} \\ f_{Ab} & f_{Bb} & f_{Cb} \\ f_{Ac} & f_{Bc} & f_{Cc} \end{pmatrix} . \begin{pmatrix} v_a \\ v_b \\ v_c \end{pmatrix} \qquad [4.26]$$

Next, we factorize the matrix G, as in the case of the three-phase inverter, and we note that the voltages (v_a, v_b, v_c) form a direct balanced system, giving us an expression of the form:

$$\begin{pmatrix} v_{aN'} \\ v_{bN'} \\ v_{cN'} \end{pmatrix} = \frac{2V_{\max}}{3} C_{32} C_{32}^t . \begin{pmatrix} f_{Aa} & f_{Ba} & f_{Ca} \\ f_{Ab} & f_{Bb} & f_{Cb} \\ f_{Ac} & f_{Bc} & f_{Cc} \end{pmatrix} . C_{32} . \begin{pmatrix} \cos \omega t \\ \sin \omega t \end{pmatrix} \qquad [4.27]$$

It is then possible to carry out a Clarke transformation to define the two-phase voltages applied to the load (denoted as $v_{\alpha N'}$ and $v_{\beta N'}$ and combined in a vector denoted as $\mathbf{v}_{2N'}$):

$$\mathbf{v}_{2N'} = \frac{2V_{\max}}{3} C_{32}^{t}. \begin{pmatrix} f_{Aa} & f_{Ba} & f_{Ca} \\ f_{Ab} & f_{Bb} & f_{Cb} \\ f_{Ac} & f_{Bc} & f_{Cc} \end{pmatrix} .C_{32}. \begin{pmatrix} \cos \omega t \\ \sin \omega t \end{pmatrix} \quad [4.28]$$

This result is visibly different from that found for a three-phase inverter, despite the fact that the equation process follows a similar approach. Note that the result is dependent on the instant because of the variable network voltages and thus of the dependences in $\cos \omega t$ and $\sin \omega t$. Furthermore, this converter offers more possible control inputs than a simple inverter; the nine switching functions defined in matrix (f_{Xy}) give us 27 authorized combinations. Figure 4.16 shows that, despite this increase in the number of degrees of freedom, the accessible zones in the plane $\alpha\beta$ are still regular hexagons (centered on the origin of the frame of reference); however, the size of these hexagons fluctuates over time. It is therefore useful to determine the least favorable case in order to assess the maximum amplitude which may be delivered to a load in permanent sinusoidal mode; this corresponds to the radius of the circle drawn in the smallest of the available hexagons. In order to remain within the linear operating zone, the amplitude of the output voltages must always be less than or equal to $\frac{\sqrt{3}}{2}$ times the amplitude of the applied input voltages (whether phase or phase-to-phase voltages).

We then need to develop PWM strategies similar to those used for inverters, notably by means of a vector-based approach.

4.5.3. *Switch commutation*

Switching in four-segment switches, such as those shown in Figure 4.13, is not as simple as switching transistors in a chopper or an inverter. When a transistor opens in these converters, a free wheel diode switches on spontaneously. In a two-transistor switch, we must be able to ensure instantaneous conduction in another transistor when one transistor switches off. This is problematic, and the commutation process requires certain precautions to be taken; the process may be divided into four steps (four-step current commutation strategy [WHE 04]). This commutation is also referred to as "semi-soft" in [MOR 07]. To analyze this commutation process, we will consider the simplest possible case, using two four-segment switches to connect two voltage sources and a current source. This topology is illustrated in Figure 4.17.

Let us suppose we wish to switch from a state where (K_1, K_2) is closed (with (K_3, K_4) open) to a state where (K_3, K_4) is closed (with (K_1, K_2) open). Two cases are possible, depending on the sign of the current I_s.

Taking current I_s as positive:

1) the transistor of K_2 is opened (transparent for the system, as this transistor was not carrying a current);

2) the transistor of K_3 is closed: this does not necessarily mean that a current will immediately circulate through the component (this is dependent on the sign of $V_1 - V_2$);

3) the transistor of K_1 is then opened (this time, current I_s is guaranteed to circulate in the transistor of K_3 and the diode of K_4);

4) the transistor of K_4 is closed in order to guarantee that the current will continue to circulate even if the sign changes.

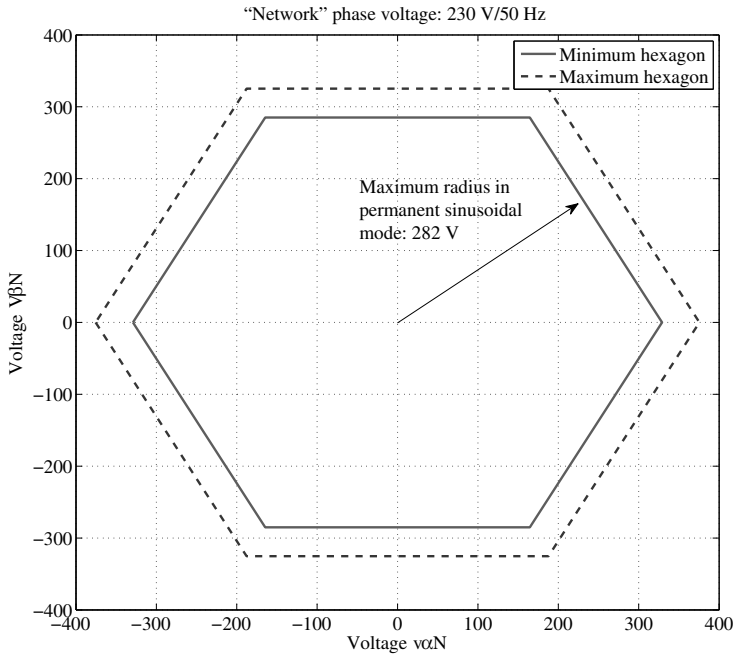


Figure 4.16. *Minimum and maximum converter output hexagons*

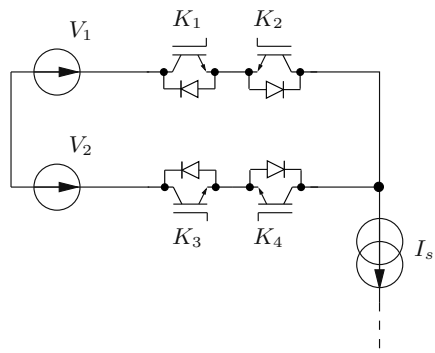


Figure 4.17. *Elementary AC-AC commutation structure*

A negative value of I_s gives the following situation:

1) the transistor of K_1 is opened (which is still transparent for the system, as the current is null);

2) the transistor of K_4 is closed;

3) the transistor of K_2 is opened;

4) the transistor of K_3 is closed.

We clearly see that four successive steps are involved in the commutation process for each situation. This is also true for switching in the opposite direction.

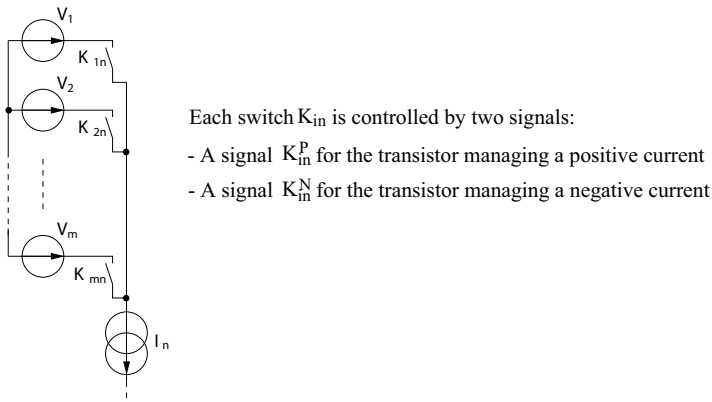


Figure 4.18. *Generic commutation structure for an output current*

The general commutation principle is shown in Figure 4.19. This is based on the structure defined in Figure 4.18. The state graph clearly illustrates the combinatory and sequential aspect of the commutation process. The preferred targets for implementing gate drive logic circuitry of a matrix converter are generally programmable logic devices, such as CPLD and FPGA.

4.5.4. *Switch protection*

A priori, safe operation is ensured by controls, using the algorithm presented in Figure 4.19. However, this safety element is based on the hypothesis that the measurement of the current I_n is reliable. This measurement is provided by a sensor (for example, a Hall effect active sensor), which may

malfunction or deliver false information due to measurement noise. Physical protection is therefore required as backup in the case of an operational safety failure in the program. To do this, the converter structure needs to include a protection device, such as a varistor, as shown in Figure 4.20. In normal operating mode, these components are “invisible”, and are only switched on in the case of overvoltage. They should be chosen with regard to the switch rating (at intermediate level, between the nominal usage voltage and the rated voltage of the switches). These components are able to dissipate moderate energy, and we must ensure that the magnetic energy stored in the load is compatible with the components used; otherwise, other alternatives should be considered, using diode rectifiers and RC circuits (see [MOR 07]).

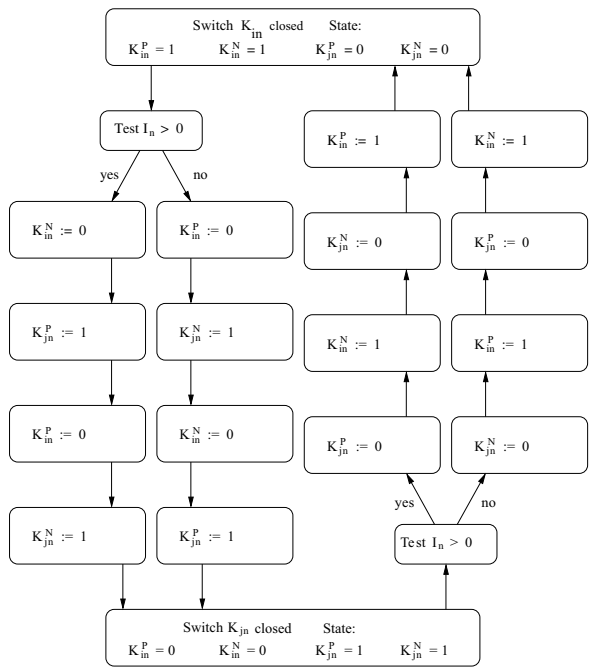


Figure 4.19. *Four-step commutation flowchart*

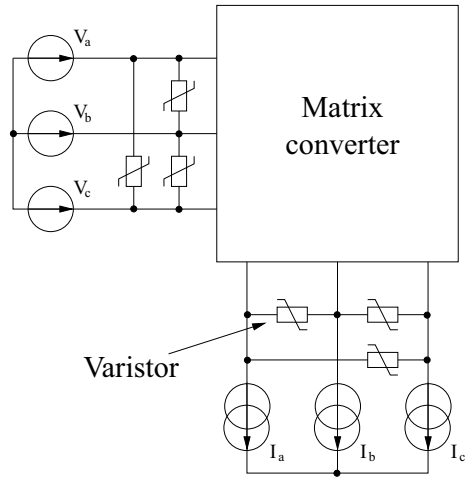


Figure 4.20. *Matrix converter protected by varistors*

5

Introduction to Multi-level Converters

5.1. Context and scope of the study

Multilevel and multicellular converters are currently the subject of extensive research activity, with a considerable number of publications in scientific journals and multiple conference papers on the subject. The primary objective of multilevel converters is to enable high voltages to be used with components with ratings which prevent the use of the converter topologies presented in Chapters 1 and 2. The basic idea is the same as for the series association of rectifier assemblies (Chapter 3), switches are used together in order to produce a high voltage on the load side. However, we do not simply synthesize high-voltage switches as substitutions for elementary switches; we also benefit from an increased number of degrees of freedom, provided by each elementary switch in the structure, to improve the performance of the converter. This notably allows us to increase the apparent switching frequency on the load side, in order to reduce harmonic distortion in the injected currents.

A variety of converter topologies have been proposed to achieve these results. As we have already seen, a strong resemblance exists between choppers and inverters, thus we will concede that this is also the case for multilevel

converters; these may be used in the context of both direct current (DC)/DC and DC/alternating current (AC) conversion. In this context, we will analyze the operation of different multilevel half-bridge topologies, which are used as the building blocks for four-quadrant choppers and three-phase inverters (higher numbers of phases may also be used).

Converter structures may be divided into three distinct families:

– cascaded power converters (galvanic isolation on either the “load side” or the “source side”;

– diode-clamped cells;

– imbricated cells.

This chapter is not intended to provide an exhaustive presentation of these structures and the associated control approaches, but simply to highlight the advantages and drawbacks of this type of converter, and to present elements of control approaches. We will identify control principles which are common to classic converters, as seen in the previous chapters, alongside specific control methods used to overcome the difficulties associated with the exponential increase in degrees of freedom due to the use of additional switches.

5.2. Cascaded power converters

We will begin by considering cascaded structures, as this structure is closest to the converters described in previous chapters. This structure simply involves coupling classic (two-level) inverters/choppers, in order to add the voltages produced by the two components and increase the number of possible converter output voltages. A generic structure for this type of converter is shown in Figure 5.1.

Note that this multilevel converter uses multiple full H-bridge output points, associated with a series configuration. For this configuration to be possible, isolated continuous voltages are needed (denoted as V_{dc1} to V_{dc3} here). Isolated DC–DC converters must therefore be placed at each entry point to each converter. This result may be obtained in different ways (transformers with multiple secondaries followed by rectifiers and filters, single continuous voltage used to power multiple isolated DC–DC converters[1]).

Another solution consists of associating several H bridges, powered by a common continuous voltage, and coupling their outputs using transformers connected by their secondary windings (providing both galvanic isolation and voltage aggregation). This structure, as shown in Figure 5.2, is also known as a polygonal inverter [FOC 98].

These converters are not particularly difficult to control, and the same techniques used for choppers and inverters may be employed.

However, there is an obvious limitation in the use of polygonal inverters: the presence of transformers between the converter output and the load means that DC–DC conversion is not possible, and also prevents operation at low output frequencies. This solution is generally unsatisfactory for powering electrical machines requiring variable speeds (the structure shown in Figure 5.1 is preferred in this case). This type of converter is better suited to active filtering and/or stabilization/energy management functions in electrical networks at medium voltage levels (notably within *flexible AC transmissions systems* (FACTS) or *unified power flow controllers* (UPFCs)).

1 This solution is interesting, as the isolation transformers of each DC–DC converter can then be dimensioned at a high frequency (switching frequency) and not at network frequency, as in the case of the first solution (representing gains in terms of volume and mass).

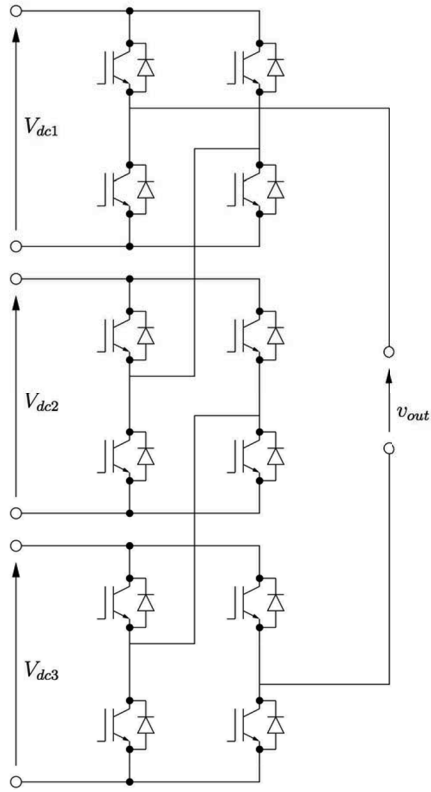


Figure 5.1. *Cascaded converter (isolated input)*

5.2.1. *Diode-clamped cells*

Compared to cascaded power converters, clamped diode cell structures present the advantage of not requiring galvanic isolation in order to operate. A pyramid structure, proposed in [YUA 00], provides a clear illustration of a generic form of *neutral point clamping* (NPC) half-bridge: this structure is shown in Figure 5.3(a).

Figure 5.3(b) shows the specific case of a three-level inverter. For this configuration, it is possible to create a table (Table 5.1) showing the possible control inputs of switches K_1, K_2, K'_1 and K'_2, with the associated output voltage values (in

this case, we presume that voltage V_{dc} is distributed equally between two capacitors C_1 and C_2, which must have identical values). This output voltage v_{out} is then denoted as the product $V_{dc}.f_m$, where f_m is a modulation function (note that this is not a binary function, as in the case of the switching functions used to model two-level inverters and choppers).

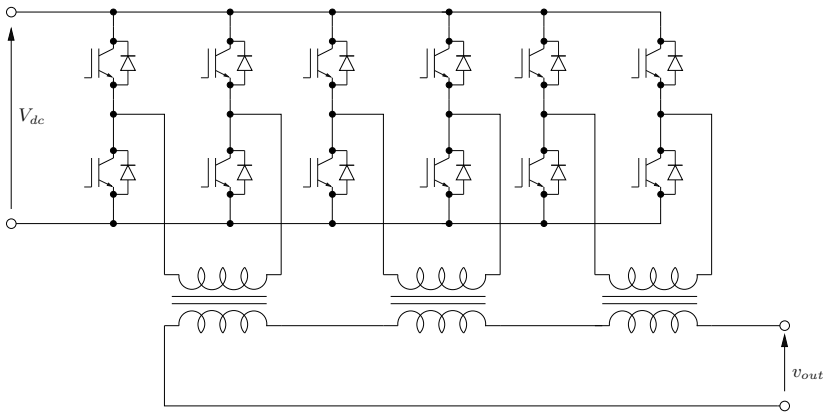


Figure 5.2. *Cascaded converter (isolated output)*

REMARK 5.1.– The modulation function is a generalization of the notion of a connection function, as seen in the previous chapters. It takes discrete values from a set of n elements for an inverter with n levels. Note that in the cases seen above, these levels are equidistant; however, this is not an absolute rule, and levels may be distributed in a non-uniform manner if required (although this is rare in practice).

Five of the possible control inputs do not require a modulation function, and thus the voltage v_{out}. In reality, the states of the diodes determine the state of the inverter. For these five cases, we therefore need to determine the obtained modulation function based on the sign of the current i_{out} in the load. These results are shown in Table 5.2. In practice, these control inputs are not desirable, as in the case of classic

inverters, where half-bridges should not be left in a fully uncontrolled state.

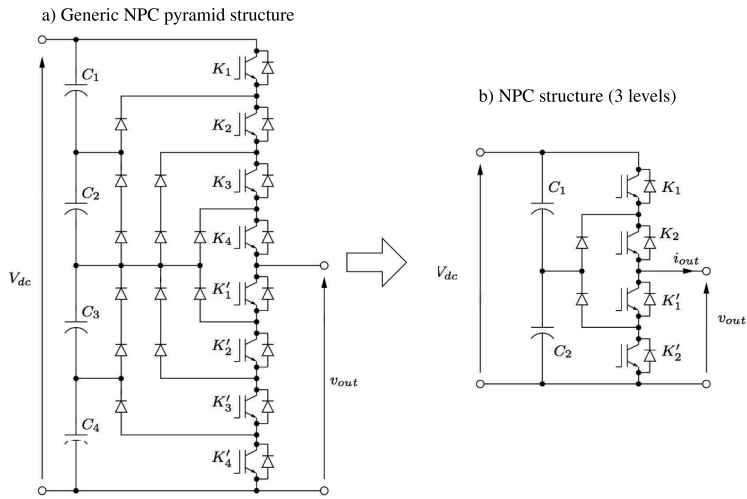


Figure 5.3. *NPC inverter: a) generic pyramid structure and b) three-level structure*

For desirable control inputs, two possibilities are systematically available for each of the three accessible values of the modulation function $(0, 1/2, 1)$. Values $f_m = 0$ and $f_m = 1$ give "unbalanced" inputs, for which three switches are open. These inputs should be avoided. The simplest solution covering all of the required cases consists of using complementary signals for K_1 and K'_1, on the one hand, and for K_2 and K'_2. This gives a simple solution, which may be summarized as follows (where ON = 1 and OFF = 0):

– $K_1 = \overline{K'_1} = 0$ and $K_2 = \overline{K'_2} = 0 \Longrightarrow f_m = 0$ and thus $v_{out} = 0$;

– $K_1 = \overline{K'_1} = 0$ and $K_2 = \overline{K'_2} = 1 \Longrightarrow f_m = 1/2$ and thus $v_{out} = V_{dc}/2$;

– $K_1 = \overline{K'_1} = 1$ and $K_2 = \overline{K'_2} = 1 \Longrightarrow f_m = 1$ and thus $v_{out} = V_{dc}$.

State of K_1	*State of* K_2	*State of* K_1'	*State of* K_2'	*Modulation function* f_m *(and* v_{out}*)*
off	off	off	off	State dependent on direction of i_{out}
off	off	off	on	State dependent on direction of i_{out}
off	off	on	off	State dependent on direction of i_{out}
off	*off*	*on*	*on*	$f_m = 0$ ($v_{out} = 0$)
off	on	off	off	State dependent on direction of i_{out}
off	on	off	on	$f_m = 1/2$ ($v_{out} = V_{dc}/2$)
off	*on*	*on*	*off*	$f_m = 1/2$ ($v_{out} = V_{dc}/2$)
off	on	on	on	forbidden configuration (short circuit of C_2)
on	off	off	off	State dependent on direction of i_{out}
on	off	off	on	State dependent on direction of i_{out}
on	off	on	off	State dependent on direction of i_{out}
on	off	on	on	$f_m = 0$ ($v_{out} = 0$)
on	*on*	*off*	*off*	$f_m = 1$ ($v_{out} = V_{dc}$)
on	on	off	on	$f_m = 1$ ($v_{out} = V_{dc}$)
on	on	on	off	forbidden configuration (short circuit of C_1)
on	on	on	on	forbidden configuration (short circuit of v_{dc})

Table 5.1. *Switch control inputs and output voltages for a three-level NPC inverter*

5.3. Imbricated cell converters

Imbricated cell or multicellular cell converters were developed by Foch and Meynard, and are presented in

[MEY 93]. The generic form of this topology is shown in Figure 5.4. The structure consists of associating classic switching cells (two transistors with antiparallel diodes); a capacitor is inserted between each imbricated cell, and a fraction of the input voltage V_{dc} of the whole converter is applied to the terminals of this capacitor. For an inverter with n cells, a voltage of V_{dc}/n will be present at the terminals of capacitor C_1 (the capacitor of the "innermost" cell, which we will denote as cell number 1, i.e. the cell connected to the load). For capacitor C_2, we have a voltage of $2V_{dc}/n$. This is then generalized with a voltage of kV_{dc}/n at the terminal of any capacitor C_k.

State of K_1	*State of* K_2	*State of* K'_1	*State of* K'_2	*Sign of* i_{out}	*Modulation function* f_m
off	off	off	off	+	0
off	off	off	on	+	0
off	off	on	off	+	0
off	on	off	off	+	1
on	off	off	off	+	0
on	off	off	on	+	0
on	off	on	off	+	0
off	off	off	off	-	1
off	off	off	on	-	1
off	off	on	off	-	1/2
off	on	off	off	-	1
on	off	off	off	-	1
on	off	off	on	-	1
on	off	on	off	-	1/2

Table 5.2. *Switch control inputs and associated connection functions*

Any cell $k > 1$ may be seen as a loop made up of two switches (K_k and K'_k) and two capacitors, C_k and C_{k-1}. If the load connected to the converter output is of the "current source" type, one of the two switches in each cell must be switched on. From this, we see that the open switch must be able to withstand the voltage difference required by the

capacitor pair, i.e. V_{dc}/n. This general result shows that the rated voltage required for each switch is inversely proportional to the number of cells used; this is particularly interesting for high voltages. However, the closer the capacitor ratings are to the converter input, the higher they will be selected to be used in this structure; capacitor C_1 will have a rated voltage equivalent to that of the switches.

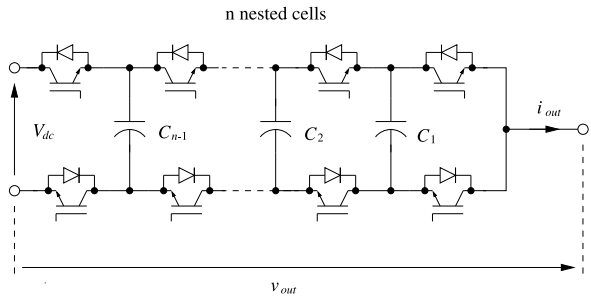


Figure 5.4. *Imbricated cell inverter*

For illustrative purposes, let us consider an example with two cells (equivalent to the NPC converter shown in Figure 5.3(b)). We have a voltage V_{dc} at the terminals of capacitor C_2, while at the terminals of C_1, the voltage has a value of $V_{dc}/2$. One switch in each cell (the upper switch, denoted as K_i for cell i, or the lower switch, K_i') must be on in order to guarantee a continuous current in the load, which we will consider to be a source of current (such as a machine winding). It is therefore reasonable to use complementary switch control inputs for each cell ($K_i' = \overline{K_i}$). We thus obtain four possible states, as shown in the diagrams of Figure 5.5.

5.4. Control structures

A significant advantage of multilevel converters lies in their ability to present a high apparent switching frequency on the load side alongside a lower effective switching frequency in the switches. This facilitates voltage filtering,

notably when the components used are slow and require a low switching frequency. This is particularly true in high-power applications (such as rail traction), using components such as high-voltage insulated-gate bipolar transistors (IGBTs) (with a rating of $V_{CE} \geq 1700\,\mathrm{V}$) or gate turn-off thyristor (GTO)/integrated gate-commutated thyristors (IGCTs).

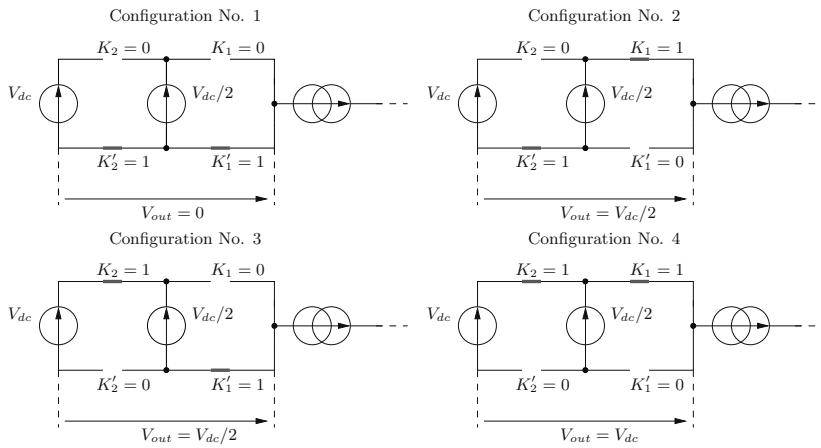


Figure 5.5. *Configurations of a two-cell imbricated inverter*

As an illustration, we will test two possible control structures for the three-level NPC inverter presented in section 5.2.1.

5.4.1. *"Unipolar" intersective PWM*

The first of these structures (as shown in Figure 5.6) consists of using two triangular carriers of frequency F_d to control the two pairs (K_1,K'_1) and (K_2, K'_2).

The first carrier, denoted as $p_1(t)$, varies between 0 and 1/2; the second, denoted as $p_2(t)$, varies between 1/2 and 1. The simplest solution consists of stating that $p_2(t) = p_1(t) + 1/2$. The two carriers are then compared to a sinusoidal modulation

signal $m(t)$ oscillating at a maximum frequency of F_m between 0 and 1. Typically, a modulation index $k_m \leq$ is defined such that:

$$m(t) = \frac{1}{2}\left(1 + k_m.\cos\left(2\pi F_m t + \varphi_m\right)\right) \qquad [5.1]$$

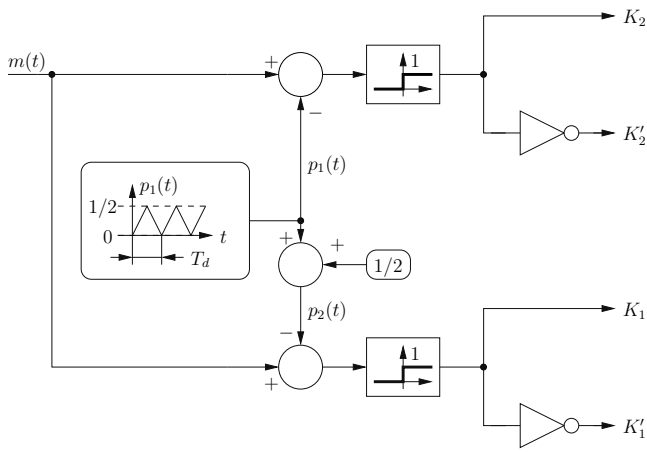


Figure 5.6. *Unipolar control scheme for an NPC inverter*

Figure 5.7 shows the waveforms of control inputs K_i and K_i' obtained using this control structure for two values of $m(t)$. We begin by applying $m = 1/4$, followed by $m = 3/4$, in order to show the two operating zones of the modulator. The modulation function is also shown, in accordance with the results presented in Table 5.2.

The waveform of the modulation function takes the form of a three-level signal, and the spectrum is therefore less rich than that produced by a two-level PWM approach at the same amplitude. However, we see that the apparent switching frequency is the same as that of the switches (frequency $F_d = 1/T_d$). A different strategy may also be used, based on interleaved carriers; this second strategy allows the apparent frequency to be increased, which consequently

improves the quality of the current injected into a load for a switching frequency required by the switches. This interleaved PWM approach will be discussed in the following section, and the two strategies will be compared in spectrum analysis terms in section 5.4.3 for the sinusoidal modulation signal given in equation [5.1].

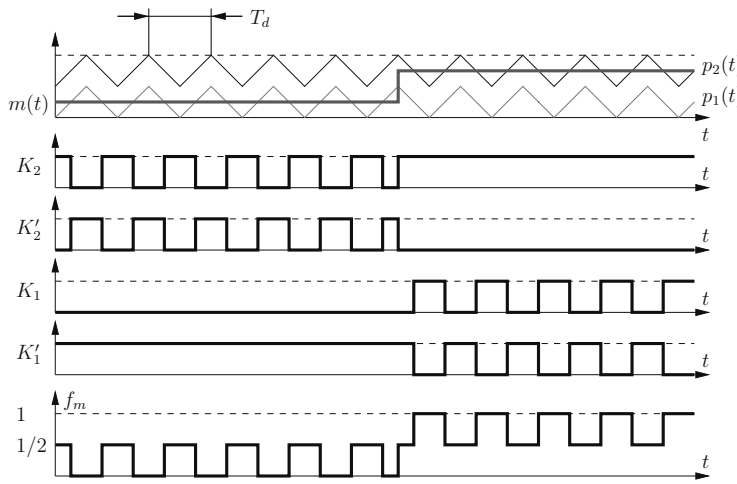


Figure 5.7. *Waveforms for a unipolar control scheme*

5.4.2. *Interleaved PWM*

Interleaved PWM techniques are not well suited to the NPC structure discussed earlier, as when switches are grouped into pairs, (K_1, K_1') and (K_2, K_2'), using complementary control, four different combinations are theoretically possible:

- $K_1 = 0$, $K_1' = 1$, $K_2 = 0$, $K_2' = 1$;
- $K_1 = 1$, $K_1' = 0$, $K_2 = 0$, $K_2' = 1$;
- $K_1 = 0$, $K_1' = 1$, $K_2 = 1$, $K_2' = 0$;
- $K_1 = 1$, $K_1' = 0$, $K_2 = 1$, $K_2' = 0$.

The second configuration leads to an unknown state (dependent on the direction of the current i_{out} injected into the load). An imbricated topology is therefore better suited to use with interleaved strategies; as we saw in section 5.3, each cell provides a contribution of $V_{dc}/2$ to the output voltage V_{out}, with no real restrictions in terms of control.

Consequently, we must simply compare the full amplitude modulator with a full amplitude carrier for each cell in order to obtain a modulation of the output voltage between 0 and V_{dc}. However, there are no constraints imposing a link between the carriers used for the two cells, with the exception of the amplitude. The two carriers may thus be "complementary", with one at its maximum value, while the other is at its minimum value. Thus, taking $p_1(t)$ as a symmetrical triangular carrier used for cell 1, with a variation fixed, by convention, between 0 and 1, cell 2 may use a carrier $p_2(t)$ expressed as:

$$p_2(t) = 1 - p_1(t) \qquad [5.2]$$

The structure of the PWM controller is shown in Figure 5.8 and the associated waveforms for the control inputs and the modulation function are shown in Figure 5.9. These illustrations use the same conditions applied in Figure 5.7, i.e. a modulating signal $m(t)$ which is constant by intervals ($m = 1/4$ followed by $m = 3/4$). We see that the apparent frequency of switching in the modulation frequency is doubled using this control scheme. In the following section, we will compare the spectrums obtained in the two cases for a sinusoidal modulator.

5.4.3. *Spectrum comparison of the two strategies*

So far, we have considered a unipolar strategy applied to an NPC inverter and an interleaved PWM strategy used with an imbricated cell inverter. From an operational perspective,

these two converters and strategies are equivalent. At spectrum level, however, the output voltage wave (or, simply, the modulation function wave) presents significant differences, even when the same switching frequency is used in the switches.

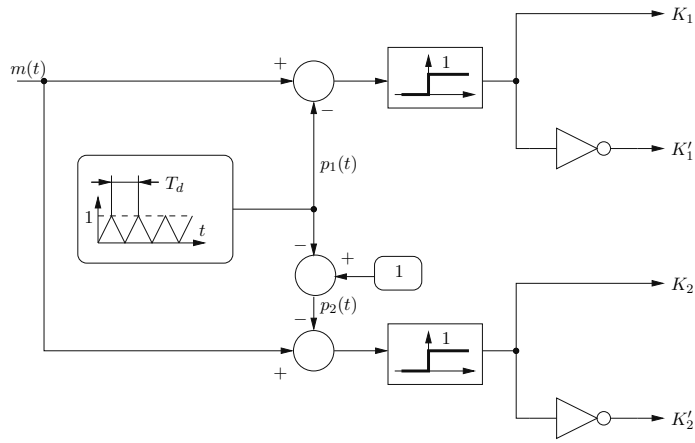


Figure 5.8. *Interleaved control signals for a two-cell imbricated inverter*

For comparison purposes, we will consider a modulating signal with the form designed by equation [5.1], taking $k_m = 0.9$ (a high-amplitude mode, but one which remains within the linear operating zone). In order to obtain a satisfactory modulation frame, we will use a ratio of $F_d/F_m = 40$. The simulated waveforms of the modulation function and the associated spectra are shown in Figure 5.10. The results of unipolar PWM are presented on the left, with interleaved PWM on the right. We clearly see that the latter strategy presents significant improvements in the spectrum of the voltage wave; the first harmonics appear at twice the switching frequency, and for a "first-order low-pass"-type load, we can expect an additional damping of $-6\,\text{dB}$ (as harmonics appear in the octave above); this represents a factor 2 reduction in the amplitude of the first current

harmonics. Moreover, we see that the group of rays at approximately 2 kHz for interleaved PWM presents a lower amplitude than the group of rays at 1 kHz for unipolar PWM (these are the first ray groups for each approach).

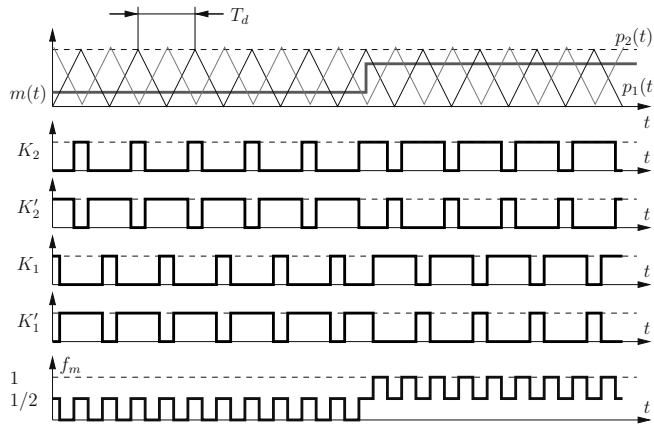


Figure 5.9. *Waveforms for interleaved control approaches*

5.4.4. *Voltage balancing*

In NPC and imbricated cell structures, intermediate voltages are supplied by capacitors and not by constant voltage sources. These voltages may therefore vary, and we need to ensure that they are balanced by means of control inputs and/or the use of auxiliary equipment.

For the NPC inverter (see Figure 5.11), we therefore need to ensure that the current arriving at the node connecting the two capacitors has an average value of zero. Note that this capacitance bridge may be shared by three NPC half-bridges for a three-phase inverter. In this context, and with a three-wire load power supply, this behavior is easier to maintain. This structure is relatively economical in terms of the improvements it provides in terms of the quality of voltages produced when compared to a two-level inverter.

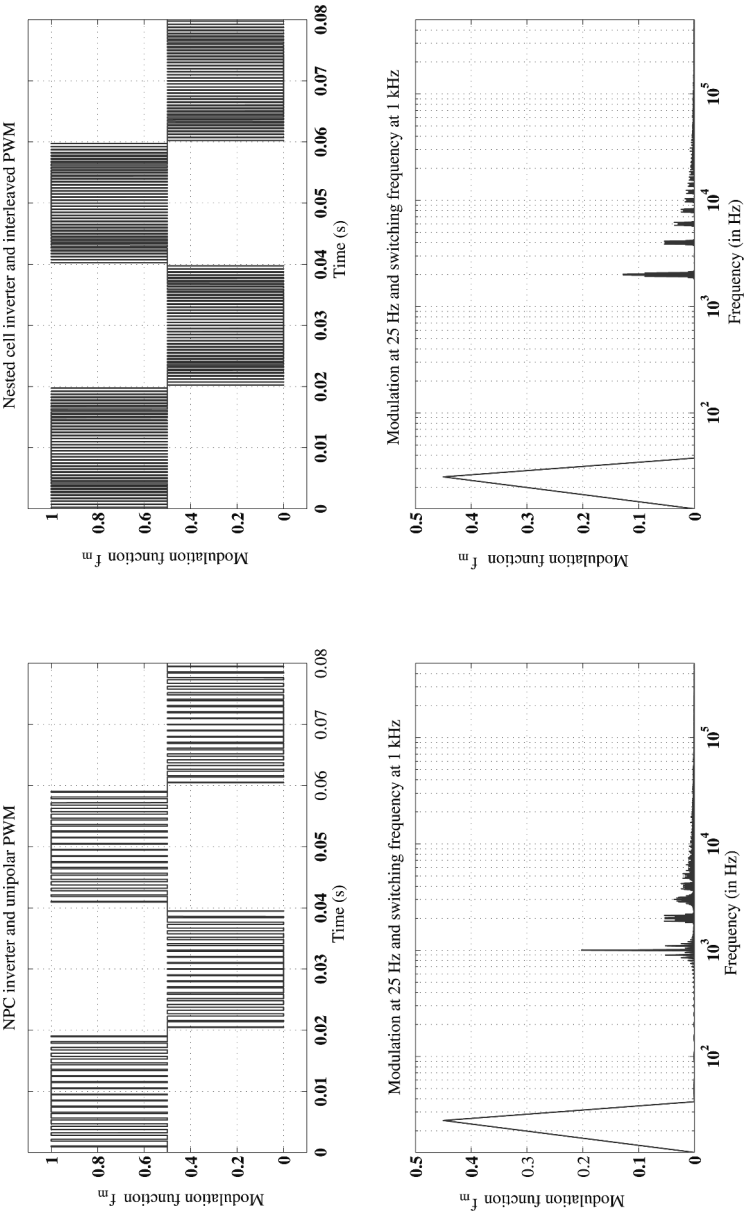


Figure 5.10. *Comparison of unipolar PWM for an NPC inverter and interleaved PWM for an imbricated cell inverter*

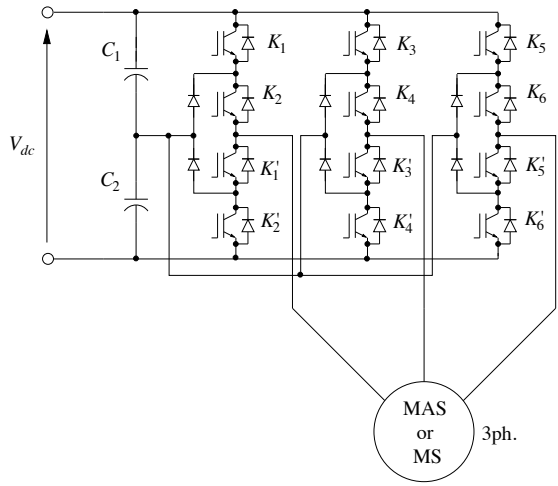


Figure 5.11. *Interconnection between two imbricated cells*

For the imbricated cell inverter, we may use the generic diagram of a cell i shown in Figure 5.12. Switches K_i and K'_i are controlled in a complementary manner[2], and we suppose that the switched current (equal to i_{out}, current injected into the load) remains constant over a switching period T_d. Consequently, switch K_i (a transistor if $i_{out} > 0$, a diode otherwise) will be traversed by this current during a time interval $\alpha_i.T_d$ (where α_i is a control input duty ratio attached to the switching cell i) while switch K'_i (a transistor if $i_{out} < 0$, a diode otherwise) will be traversed by the same current during a time interval $(1 - \alpha_i).T_d$. This allows us to write the dynamic of the sliding average voltage $\langle v_{Ci} \rangle_{T_d}$ (for a time window of duration T_d) at the terminals of capacitor C_i as follows:

$$C_i \frac{d \langle v_{Ci} \rangle_{T_d}}{dt} = \left\langle i_{K_{i+1}} \right\rangle_{T_d} - \langle i_{K_i} \rangle_{T_d} = (\alpha_{i+1} - \alpha_i) \, .i_{out} \quad [5.3]$$

2 This is also applicable to K_{i+1} and K'_{i+1}.

The voltage at the capacitor terminals will be stable if $\alpha_{i+1} - \alpha_i = 0$. This is clearly verified in the switching period if we use identical carriers for each cell, but also when the carriers are interleaved, as in the case shown in Figure 5.9. This solution is (almost) systematically chosen, due to the increase in the apparent frequency of the capacitor output. Generally speaking, n carriers are used with a phase shift of $2\pi/n$ for a converter with n imbricated cells.

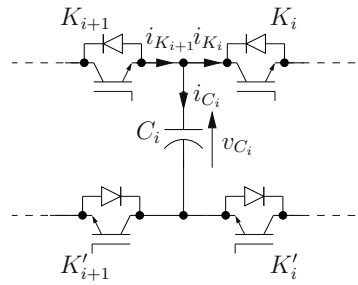


Figure 5.12. *Interconnection between two imbricated cells*

This idealized study should not be seen as an exhaustive study of the problem of voltage stabilization at capacitor terminals, and even less for the case of balancing voltages between capacitors in converters using more than two cells. While imbricated cell converters do possess natural balancing properties, readers interested in this specific issue in the context of these converter topologies may wish to consult some of the diverse publications on the subject, for example [SHU 11].

5.5. Note on vector PWM

Vector PWM techniques may also be applied to multilevel inverters. The main difficulty associated with this type of converter lies in the increased complexity of control due to increases in the number of degrees of liberty. However, a Clarke or Concordia transformation may be used to produce a

constellation of points instantaneously accessible in the plane $\alpha\beta$. In the case of our three-level inverter, we may write:

$$\mathbf{v}_{3M} = V_{dc}.\mathbf{f}_{m3} \qquad [5.4]$$

where $\mathbf{v}_{3M}$ is the vector of the inverter output voltages, referenced in relation to the negative terminal of the input voltage source (as with voltage V_{out} in the single-phase diagrams in Figure 5.5). $\mathbf{f}_{m3}$ is the vector of the modulation functions applied to each of the single-phase inverters making up the three-phase inverter. Note that these modulation functions take values of 0, 1/2 and 1 for this three-level inverter.

From this point on, the equation structure is entirely conventional; if we wish to determine the expressions of the phase voltages applied to the load (i.e. with regard to the real or virtual neutral of the load), we must suppose that the load is balanced, and that we have:

$$v_{aN} + v_{bN} + v_{cN} = 0 \qquad [5.5]$$

where a, b and c are the phases of the load and N is the neutral of the load.

Consequently, the equation model produces the same result as obtained for a two-level inverter:

$$\mathbf{v}_{3N} = \frac{V_{dc}}{3} \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} .\mathbf{f}_{m3} \qquad [5.6]$$

except for the fact that the control input vector is no longer composed of binary variables (0 or 1). For each component, we have three possible values, giving a total of $3^3 = 27$ possible combinations for the control input vector. We must then consider the way in which these combinations affect the voltages instantaneously available in the plane $\alpha\beta$. To do

this, we simply use a Concordia transformation (for a zero sequence component of zero):

$$T_{32}.\mathbf{v}_{2N} = V_{dc}.T_{32}.T_{32}^{t}.\mathbf{f}_{m3} \qquad [5.7]$$

Thus, multiplying this equality from the left by T_{32}^{t}, we obtain:

$$\mathbf{v}_{2N} = V_{dc}T_{32}^{t}.\mathbf{f}_{m3} \qquad [5.8]$$

Note that these Concordia components do not retain the amplitudes of the real three-phase values, and have an amplitude which is $\sqrt{3/2}$ times higher. Once this result has been established (the result is, in fact, the same as that obtained for the two-level three-phase inverter), we may produce an exhaustive list of voltages available in the plane $\alpha\beta$ (see Figure 5.13).

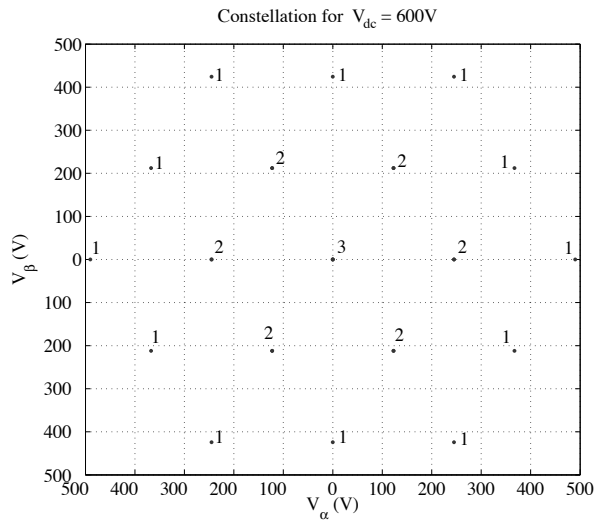


Figure 5.13. *Constellation of instantaneous voltages in the plane $\alpha\beta$ for $V_{dc} = 600\,V$*

We immediately see that the number of points in the constellation of available voltages (19) is lower than the

number of control inputs available for the inverter (27). This was also the case for the two-level inverter, where two of the input combinations produced a null vector; in this new converter, we encounter more duplication. The number of control inputs associated with each point is shown in the constellation.

6

Case Study – The Variable Speed Drive

6.1. Objective

This chapter is a case study of a full converter used to control a three-phase electrical machine, either synchronous or asynchronous. For the purposes of this study, we shall only consider the power components (including filtering and braking apparatus) and the gate drivers used to control switches (IGBT). The overall structure under consideration was presented in Figure 1.1 of Volume 1 [PAT 15a], Chapter 1.

Before beginning this study, a specification characterizing the power source and the load should be defined:

– source: three-phase network at $230/400\,\mathrm{V}$ – $50\,\mathrm{Hz}$;

– load: bipolar synchronous machine with non-salient poles, $230\,\mathrm{V}$ per winding, $3\,\mathrm{kW}$, all losses are neglected: $\cos\varphi = 0.9$[1].

1 For the purposes of this study, we shall presume that the machine windings present negligible resistance in comparison to the inductance. Moreover, we shall limit ourselves to linear modeling of the machine (i.e. a Behn–Eschenburg model).

We shall presume that the load and the converter must be able to withstand transitory operation at a power of $6\,\text{kW}$ for $10\,\text{s}$. As we wish to avoid energy being returned to the network, a diode rectifier is entirely suitable; after filtering, a brake chopper is used to dissipate the energy sent back to the DC bus by the three-phase inverter connected to the machine.

As the source and the load are imposed, we first need to verify their adequacy. Secondly, we shall design the inverter and analyze the gate driver technologies which are currently available on the market. We shall then consider rectification and filtering of the DC bus voltage. To conclude the electrical aspect of the study, we shall calculate the parameters of the brake chopper and the way in which it is controlled.

Following on from this (idealized) electrical study, the losses associated with the switches shall be considered, leading to a thermal modeling of the assembly in order to design an appropriate cooling system (covering both permanent and transitory modes).

6.2. Adequacy of the source/load

6.2.1. *Source and rectifier*

As a three-phase network is used to power the variator, a PD3 rectifier is the natural choice. This is a non-controlled (diode) rectifier; based on the results established in Chapter 3, we know that the average output voltage $\langle V_{rec} \rangle$ is expressed as:

$$\langle V_{rec} \rangle = 2V_{\max}\frac{q}{\pi}\sin\left(\frac{\pi}{q}\right) \qquad [6.1]$$

where $V_{\max}$ is the amplitude of the phase voltages and q the number of phases. In this case, we have:

$$\begin{cases} V_{\max} = 230\sqrt{2}\ [\mathrm{V}] \\ q = 3 \end{cases} \qquad [6.2]$$

We thus obtain an average rectifier output voltage of $538\,\mathrm{V}$. We presume that the voltage after LC filtering (at the inverter input point) is strictly constant, and almost equal to this value.

6.2.2. *Inverter and load*

From the results established in Chapter 2, we know that, if the DC bus voltage is U_0, the maximum amplitude of the phase voltages supplied to the load is $\frac{2}{\pi}U_0$ for "full-wave" control, and $\frac{U_0}{\sqrt{3}}$ for linear vector PWM (i.e. without overmodulation). Given that our load requires phase voltages of $230\,\mathrm{V_{RMS}}$, the inverter must be able to supply voltages with an amplitude of $230\sqrt{2} = 325\,\mathrm{V}$. In the case of full-wave PWM, this implies that the minimum voltage in the DC bus should be $510\,\mathrm{V}$; if we wish to avoid overmodulation in the inverter (i.e. to remain within the limits of linear PWM), a voltage of $563\,\mathrm{V}$ is required.

6.2.3. *Summary*

Our calculations show that the source and the load are suitable to be used together, based on the rectifier/inverter association alone. Clearly, the inverter cannot be used solely in PWM, and overmodulation is necessary to attain the maximum voltage amplitude required by the load, but we do not require any additional elements. If the voltages for this source and this load were not suited to be used together, an additional element would need to be inserted into the conversion chain. This might be:

– a transformer at the rectifier input point;

– a buck or boost converter on the DC bus (between the rectifier and the inverter).

Another possibility would be to place a transformer between the inverter and the machine, but this is not desirable, as it would complicate couple and/or speed control of the machine. Moreover, the transformer would need to be suited to operations at variable frequency (generally not the case for classic 50 or 60 Hz transformers[2]).

6.3. Inverter

6.3.1. *Current/voltage characteristics*

In the previous section, we established that the DC bus voltage is 538 V. This allows us to calculate the voltage levels which the transistors and diodes in the inverter must be able to withstand. In practice, a safety coefficient of 2 is applied in order to guarantee continued successful operation even during switching, when overvoltages may briefly occur at component terminals. Under these conditions, the transistors and diodes used must be able to withstand a minimum of 1 076 V. In practice, the standard IGBT voltage ratings are 600 and 1 200 V. Clearly, switches with a rated voltage of 600 V leave insufficient margin, so 1 200 V components should be used. The most suitable technology for this voltage and power range is IGBT. At this point, we need to characterize the rated current in order to select components (which may be integrated into a full "three-phase inverter" module, potentially including the rectifier and the brake chopper).

To do this, we begin by calculating the current which needs to be injected into the load, based on the characteristics

2 Although, theoretically speaking, this would be entirely possible.

laid out in the introduction. We know that the inverter must be able to supply $3\,\mathrm{kW}$ in permanent mode and $6\,\mathrm{kW}$ for periods of $10\,\mathrm{s}$. For the switches, it is best to assimilate the $10\,\mathrm{s}$ in transient mode to a permanent mode, due to the low thermal inertia of components; the components will therefore be designed for this transient mode (although this will not be the case for other components, such as the heatsink or the smoothing choke):

$$P = 3V.I.\cos\varphi \qquad [6.3]$$

Taking $V = 230\,\mathrm{V}$, $\cos\varphi = 0.9$ and $P = 6\,\mathrm{kW}$, we obtain:

$$I = 9.66\mathrm{A} \qquad [6.4]$$

This gives us a current with an amplitude of up to $I_{\max} = 13.7\,\mathrm{A}$.

In terms of switch design, the most important parameter depends on the technology used. For a MOSFET, which presents a resistive behavior in the ON state, it is important to evaluate the effective value of currents, as conduction losses $P_{\mathrm{cond}}^{\mathrm{MOS}}$ take the form $R_{\mathrm{DSon}}.I_{\mathrm{RMS}}^2$. IGBTs present not only dynamic resistance R_d^T but also a voltage dropoff V_{TO} when switched on, independently of the current. In these conditions, the conduction losses are expressed as:

$$P_{\mathrm{cond}}^{\mathrm{IGBT}} = V_{TO}.\langle I\rangle + R_d^T.I_{\mathrm{RMS}}^2 \qquad [6.5]$$

where $\langle I\rangle$ is the average current circulating in the switch.

Therefore, not a single parameter exists which may be used for selecting a rated current (which is subject to essentially thermal limitations). Manufacturers specify a permanent nominal current for components, corresponding to a maximum acceptable loss level. Our device needs to operate using variable currents: for this reason, we will consider a

"hybrid" parameter for rating selection, based on the following simplifying hypotheses:

– operation with a unitary power factor (load);

– design based on the inverter operating in full-wave mode.

This second hypothesis is relatively restrictive. A high safety margin should be used with regards to losses. In this case, losses are practically limited to conduction losses (with only two switching operations per fundamental period and per half-bridge); when using PWM, switching losses must also be taken into account.

It is then easy to calculate the average current and the effective current in a transistor[3], insofar as this corresponds to a half-wave rectification waveform. Thus:

$$\langle I \rangle = \frac{1}{2\pi} \int_0^{\pi} I_{\max}.\sin\theta.d\theta = \frac{I_{\max}}{\pi} \qquad [6.6]$$

and:

$$I_{\mathrm{RMS}} = \sqrt{\frac{1}{2\pi} \int_0^{\pi} I_{\max}^2 \sin^2\theta.d\theta}$$

$$= \sqrt{\frac{I_{\max}^2}{4\pi} \int_0^{\pi} (1 - \cos 2\theta)\,.d\theta} = \frac{I_{\max}}{2} \qquad [6.7]$$

A possible component choice criterion thus consists of calculating the corresponding losses for currents specified in manufacturer documentation, labeled $P_{\mathrm{cond}}^{\mathrm{ref}}$, then calculating losses [6.5] using the average and effective current losses

3 With a unitary power factor and using full-wave modulation, the diodes never enter into conduction.

established in [6.6] and [6.7]. We then apply a safety coefficient K to determine the design criterion:

$$P_{\text{cond}}^{\text{IGBT}} \geq K.P_{\text{cond}}^{\text{ref}} \qquad [6.8]$$

A coefficient of order 10 is used: note that this coefficient is applied to the power, and not to the current. Moreover, as the reference power is dissipated in "static" mode, a considerable margin is required for switching losses, as we shall see below. The safety margin $K = 10$ corresponds to a considerably lower coefficient in terms of current.

For the purposes of our case study, let us verify that the Semikron SKiiP12AC126V1 module is suitable for our application. Based on the datasheet available at www.semikron.com, the IGBT modules withstand $22\,\text{A}$ in permanent mode at 70°C (this is *a priori* the running surface temperature for a junction temperature of 125°C): a characteristic $I_C(V_{CE})$ is supplied (shown in Figure 6.1).

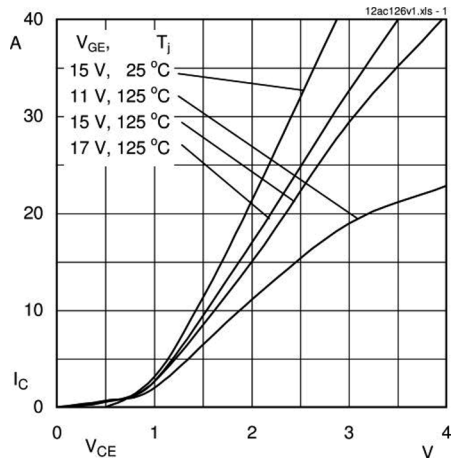


Figure 6.1. *Graph $I_C(V_{CE})$ – Semikron documentation*

Using this graph, we may evaluate the reference power dissipated by the transistor during conduction:

$$P_{\text{cond}}^{\text{ref}} = 2,5\,[\text{V}] \times 22\,[\text{A}] = 55\,[\text{W}] \qquad [6.9]$$

For our application, we know that the maximum current is $13.7\,\text{A}$. At 125°C, the transistor parameters are:

$$\begin{cases} R_d^T = 75\,\text{m}\Omega \\ V_{TO} = 0.75\,\text{V} \end{cases} \qquad [6.10]$$

Hence:

$$P_{\text{cond}}^{\text{IGBT}} = 6.79\,\text{W} \qquad [6.11]$$

There is a ratio of 8:1 between the reference power and the power which is actually dissipated during conduction by our application, giving a considerable safety margin.

This preliminary calculation may be seen as the first step in establishing a "loss budget", where $12.4\,\%$ of the available resource is allocated to effective conduction losses. Allocations should also be made for switching losses and for the safety margin. As the "small" module discussed above appears to be sufficient for our requirements, we shall continue our study using this element.

6.3.2. *Switching frequency*

The switching frequency F_d should be chosen based on a compromise between the quality of the power supply to the load (minimization of HF currents by increasing the switching frequency) and switching losses introduced into components (which may be considered to be proportional to the switching frequency).

It is relatively easy to calculate losses in IGBT transistors compared to MOSFETs, as constructors (particularly

Semikron) specify switching losses for switch-on E_{ON} and switch-off E_{OFF} (noted W_{ON} and W_{OFF} in certain other manufacturer datasheets). These values (noted in mJ) are specified for reference values of switched voltages V_{ref} and currents I_{ref}; the latter do not necessarily correspond to the values in the target application (voltage and current noted V_{app} and I_{app} respectively). This data is adapted using a simple proportionality rule:

$$E_{ON}^{\text{app}} = \frac{V_{\text{app}}.I_{\text{app}}}{V_{\text{ref}}.I_{\text{ref}}} \cdot E_{ON} \text{ and } E_{OFF}^{\text{app}} = \frac{V_{\text{app}}.I_{\text{app}}}{V_{\text{ref}}.I_{\text{ref}}} \cdot E_{OFF} \qquad [6.12]$$

In practice, as the inverter is powered using a constant voltage U_0, we may consider that the voltage V_{app} is a constant ($V_{\text{app}} = U_0 = cte$). However, the switched current is assumed to be sinusoidal. Classic PWM strategies (such as sinusoidal or vector PWM) consist of provoking switching in one half-bridge of the inverter twice per switching period, $T_d = 1/F_d$. These strategies all produce the same results in terms of switching losses (P_{com}). We may write that, generally:

$$P_{\text{com}} = 3 \cdot \frac{E_{ON} + E_{OFF}}{T_m} \cdot \frac{V_{\text{app}}}{V_{\text{ref}}.I_{\text{ref}}} \sum_{k=1}^{N} |i_a\,(k.T_d)| \qquad [6.13]$$

where T_m is the fundamental period of the sinusoidal voltages supplied to the load, and N the number of switching periods per fundamental period (i.e. $N = T_m/T_d$). Clearly, this equation covers the total losses in the converter, as it includes the factor 3 at the beginning of the expression. In this case, we assume that the chosen strategy balances the three half-bridges (this is true for the cited strategies, and is normally valid for all strategies used in practice). Consequently, our calculations are carried out using current i_a alone (the choice of phase a is arbitrary).

Assuming that the number of switching periods within the fundamental period is sufficiently high, it is possible to substitute the following integral for the discrete sum:

$$P_{\text{com}} = 3 \cdot \frac{E_{ON} + E_{OFF}}{T_d.T_m} \cdot \frac{V_{\text{app}}}{V_{\text{ref}}.I_{\text{ref}}} \int_0^{T_m} |i_a(t)| .dt \qquad [6.14]$$

We then change a variable, taking $\theta = \omega_m t$, where $\omega_m = 2\pi F_m$, and we obtain:

$$P_{\text{com}} = \frac{3}{2\pi} \cdot \frac{E_{ON} + E_{OFF}}{T_d} \cdot \frac{V_{\text{app}}}{V_{\text{ref}}.I_{\text{ref}}} \int_0^{2\pi} |i_a(\theta)| .d\theta \qquad [6.15]$$

Finally, supposing that the current i_a is purely sinusoidal with amplitude $I_{\max}$, we obtain:

$$P_{\text{com}} = \frac{6}{\pi} \cdot \frac{E_{ON} + E_{OFF}}{T_d} \cdot \frac{V_{\text{app}}.I_{\max}}{V_{\text{ref}}.I_{\text{ref}}} \qquad [6.16]$$

In our case study, if we wish to eliminate any risk of acoustical disturbance induced by the "converter/machine" system, a switching frequency of $20\,\text{kHz}$ ($T_d = 50\,\mu\text{s}$) would be ideal, if this choice is reasonable with regard to switching losses. Generally speaking, this is not problematic at relatively low power levels, as in this case. However, at high power levels (such as for rail traction) this choice may be critical; the slower switches used in these cases are not able to tolerate high-frequency switching.

In our case, considering the SKiiP12AC126V1 module, parameters E_{ON} and E_{OFF} take the following values:

$$\begin{cases} E_{ON} = 1.7\,\text{mJ} \\ E_{OFF} = 1.9\,\text{mJ} \end{cases} \qquad [6.17]$$

These values are specified in the datasheet for a reference voltage V_{ref} of 600 V and a current I_{ref} of $15\,\text{A}$. Taking the least

favorable case in terms of current amplitude ($I_{\max} = 13.7\,\text{A}$ for transitory mode, over $10\,\text{s}$ @ $6\,\text{kW}$), we obtain:

$$P_{\text{com}} = 112.6\text{W} \qquad [6.18]$$

Note that the DC bus voltage is $538\,\text{V}$, and that this value represents the total switching losses in the inverter.

REMARK 6.1.– We have seen that operating at maximum amplitude only occurs in cases of overmodulation (or in full-wave mode). However, it is wise to evaluate losses on the basis of linear PWM operation.

As the calculated power is dissipated in the whole inverter, we may evaluate transistor losses at 18.77 W. The first observation to make is that switching losses represent a significant part of the overall losses in the transistor. Note, however, that we have not considered losses in the diodes; in cases of operation with PWM switching, diodes must necessarily be in a state of conduction during certain phases. However, this calculation provides a good approximation of real losses: this point will be developed further in section 6.5.1. Note that this choice of module is coherent with the typical application indications ($5.5\,\text{kW}$ machine) given on the first page of the module documentation.

REMARK 6.2.– The decision to use a power module when designing a full variable speed drive is not only based on the simplicity and robustness of connections, but also on the choice of components. The diodes associated with IGBTs are perfectly suited to the target application, and so their rating does not need to be determined.

6.3.3. *Gate drivers*

As we saw in Chapter 4 of Volume 1 [PAT 15a], an IGBT/MOSFET gate driver is required. This kind of device injects currents of the order of one ampere (or more) into

transistor gates to ensure rapid switching. In the case of converters using half-bridges with "high" side transistors (choppers or inverters), we encounter an additional problem concerning the control of the voltage V_{GE} (the voltage between the gate and the collector of an IGBT, responsible for switch-on and switch-off), as the emitter has a floating potential.

As we have seen, various solutions exist, with varying levels of integration, performance and cost. The most widespread (and cheapest) option consists of "building" a floating power supply with a diode pump. This element includes a diode, used with a bootstrap capacitor, which provides small-scale energy storage. Floating power supplies for gate control in MOSFET or IGBT transistors do not need to be particularly powerful, as gate control is non-dissipative: once switched on or off, no power is required in the component gates. This means that a simple load transfer from a capacitor to the transistor gate is sufficient.

Note, however, the limitations of this type of gate control:

– the bootstrap capacitor voltage is only quasi-constant if its capacitance is high in relation to that of the transistor gate to power;

– the bootstrap capacitor voltage must be recycled regularly to compensate for self-discharge in the capacitor (current leakage).

We therefore need to evaluate the capacitance of the transistor gate in order to choose a capacitor with a value at least ten times (and preferably one hundred times) higher. Moreover, we must ensure that half-bridges switch with sufficient regularity; this means that modulator saturation should be avoided, or at least take place for controlled durations. This problem is generally not critical for inverters used to modify duty ratios in fundamental periods which are often relatively short when overmodulation occurs (full

wave = overspeed). However, hysteresis control of a chopper can prevent a driver of this type from working at all.

The capacitance of a transistor gate is generally evaluated by observing the characteristic $V_{GE}(Q_G)$, which shows the load required to attain a sufficient gate voltage for transistor control. This curve, shown in Figure 6.2 for the SKiiP 12AC126V1 module, shows that a load of around $108\,\mathrm{nC}$ is required for satisfactory control of transistors at $15\,\mathrm{V}$.

Consequently, if we use a capacitor with an initial load of $15\,\mathrm{V}$, it must be able to provide $Q = 108\,\mathrm{nC}$, limiting, for example, the voltage dropoff at $\Delta U = 2\,\mathrm{V}$[4]. In this way, we can calculate the required bootstrap capacitance C_{boot}:

$$C_{\mathrm{boot}} = \frac{Q}{\Delta U} = 54\,\mathrm{nF} \qquad [6.19]$$

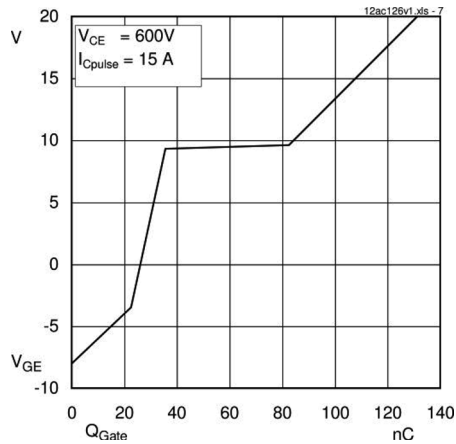


Figure 6.2. *Graph $V_{GE}(Q_G)$ – Semikron documentation*

The required capacitance is thus relatively low. It is best to increase this value by a factor of ten, or even one hundred,

4 This guarantees control will take place without reducing efficiency with regard to the power circuit.

which can generally be done without the size of the capacitor becoming problematic: a non-polarized capacitor of $1\,\mu$F withstanding $15\,$V has a volume of less than $1\,\mathrm{cm}^3$.

REMARK 6.3.– Note that the gate capacitance of the transistor in question is particularly low (of the order of an nC) and that the characteristic $V_{GE}(Q_G)$ begins by applying a negative voltage V_{GE} (switch-off zone).

To complete the design of gate driver circuitry, we generally need to calculate the resistance placed between the driver and the transistor gate (MOSFET or IGBT). A simple method may be used to approximately evaluate switching time as a function of this resistance. By fixing a value for the switching time, we may therefore determine the appropriate resistance. We may also wish to limit the current injected into the gate in response to the limitations of the driver. In this case, the issue does not arise, as the manufacturer specifies a required gate resistance: $R_{G\mathrm{on}} = R_{G\mathrm{off}} = 30\,\Omega$[5] (we can verify that using $15\,$V, the pulse current injected into the gate will never exceed $0.5\,$A).

6.4. Rectifier and filter

6.4.1. *Behavior of the rectifier*

We have already seen that, in our application, the average rectifier output voltage is $538\,$V. We can also calculate the peak-to-peak ripple of the voltage directly at the rectifier (PD3 type) output point, following the waveforms established in Chapter 3:

$$\Delta V_{rec} = V_{\max}\sqrt{3}\left(1-\cos\left(\frac{\pi}{6}\right)\right) = V_{\max}\sqrt{3}\left(1-\frac{\sqrt{3}}{2}\right) \qquad [6.20]$$

5 It is possible to differentiate between the gate resistances used in switch-on and switch-off (using current directing diodes), although this is not necessary here.

In this case, we obtain:

$$\Delta V_{rec} = 75.5\text{V} \qquad [6.21]$$

To guarantee a voltage ripple of the order of $\pm 1\,\%$ at the inverter input point, the ripple needs to be reduced to $10.8\,\text{V}$ peak-to-peak, i.e. a reduction by a factor of 7 (around $17\,\text{dB}$).

In parallel, we also wish to smooth the current delivered by the rectifier. We shall base our approach on the filtering study in Chapter 3, but this time for a three-phase rectifier. Firstly, we must calculate the average current $\langle I_{rec} \rangle$ which will be supplied by the rectifier; in this case, we use the case of permanent mode, with a load (machine) of $3\,\text{kW}$. In this case, the inverter is presumed to be ideal, so we consider that the power P_{rec} provided by the rectifier is also of $3\,\text{kW}$. Hence:

$$\langle I_{rec} \rangle = \frac{P_{rec}}{\langle V_{rec} \rangle} = \frac{3\text{kW}}{538\text{V}} = 5.58\text{A} \qquad [6.22]$$

We may, therefore, choose to maintain a peak-to-peak current ripple of the order of $10\,\%$ of the average value (for example), in this case, $558\,\text{mA}$.

6.4.2. *Choke dimensioning*

We now need to determine the instants (or angles) at which the instantaneous rectified voltage $v_{rec}(\theta) = V_{\max} \cos\theta$ exceeds the average value $\langle V_{rec} \rangle$:

$$\theta_{1/2} = \pm \arccos\left(\frac{\langle V_{rec} \rangle}{V_{\max}\sqrt{6}}\right) = 0.301\,\text{rad i.e. } 17.3° \qquad [6.23]$$

Next, we calculate the ripple Δi_L of current i_L in the choke, taking:

$$\Delta i_L = \frac{1}{L\omega} \int_{\theta_1}^{\theta_2} \left(v_{rec}\left(\theta\right) - \langle V_{rec} \rangle\right) .d\theta \qquad [6.24]$$

hence:

$$L = \frac{1}{\Delta i_L \omega} \int_{\theta_1}^{\theta_2} \left(v_{rec}\left(\theta\right) - \langle V_{rec} \rangle \right) .d\theta = 58\,\mathrm{mH} \qquad [6.25]$$

A choke of $58\,\mathrm{mH}$ is therefore required, and should not saturate (even in transitent mode at $6\,\mathrm{kW}$, i.e. with a current of $11.2\,\mathrm{A}$).

6.4.3. *Capacitance calculation (rectifier)*

We have established that the voltage ripple (at $300\,\mathrm{Hz}$ for a $50\,\mathrm{Hz}$ network) at the filter output point needs to be reduced by $17\,\mathrm{dB}$. It is arguably safer, and simpler, to work with a reduction of $20\,\mathrm{dB}$ (factor 10). To do this, we note that our LC filter presents a 2^{nd} order behavior, with an eigenfrequency:

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \qquad [6.26]$$

The reduction slope is $-40\,\mathrm{dB/decade}$ for this type of filter, so a half-decade will be sufficient to produce a factor 10 ripple reduction, on the assumption that this is purely sinusoidal at $300\,\mathrm{Hz}$ (this simplifying hypothesis was also used in Chapter 3). The resonant frequency of the filter should therefore be placed a half-decade lower than the frequency of the ripple; a half-decade corresponds to a factor of $10^{1/2} = \sqrt{10} = 3.16$. We therefore take:

$$f_0 = \frac{300}{3.16} = 94.9\ [\mathrm{Hz}] = \frac{1}{2\pi\sqrt{LC}} \qquad [6.27]$$

As we have already calculated the value of L required to satisfy the ripple criterion for the current supplied by the rectifier, we simply need to determine the required capacitance:

$$C = 48.5\,\mu\mathrm{F} \qquad [6.28]$$

6.4.4. *Inverter/capacitor interactions*

The capacitor calculations above were based purely on filtering the ripple of the voltage produced by a diode rectifier placed upstream. Unfortunately, this capacitor is also subject to current stress imposed by the inverter, placed downstream. In certain applications, this represents the most limiting aspect of the problem, and this element needs to be dealt with in order to ensure correct dimensioning of the overall converter.

We shall begin by calculating the reactance produced by L at $20\,\text{kHz}$ (switching frequency used by the inverter):

$$X_L = L.\omega = 2\pi L.F_d = 7.29\,\text{k}\Omega \qquad [6.29]$$

In the same way, we can evaluate the reactance introduced by C at the same frequency:

$$X_C = -\frac{1}{C\omega} = -0.164\,\Omega \qquad [6.30]$$

In a three-phase inverter, the current drawn from the DC bus is purely constant in the LF (low frequency) domain, as the fluctuating power is null[6]. Consequently, the chopped current entering the inverter only includes HF components located around the switching frequency and multiples of this frequency.

As we have seen, there is a considerable difference between the reactances of the capacitor and the inductance at $20\,\text{kHz}$ (this difference is even greater at higher frequencies). In this case, the HF current drawn from the DC bus by the inverter can only circulate in the capacitor. We must ensure that the voltage ripple remains low (the effect is added to that produced by the rectifier), but also take account of the

6 This is not the case in a single-phase structure.

nominal operating current of the capacitor (from manufacturer data), which must be lower than the current imposed by the inverter.

For APWM strategies using two adjacent active vectors during each switching period (sine PWM and classic vector PWM, as seen in Chapter 2, the effective current $RMS\,(I_c)$ in the capacitor may be expressed in analytical form in the following manner:

$$RMS\,(I_c) = I_{\max}.\sqrt{\frac{\sqrt{3}m}{4\pi} + \left(\frac{\sqrt{3}m}{\pi} - \frac{9m^2}{16}\right)\cos^2\varphi} \quad [6.31]$$

where $I_{\max}$ is the amplitude of currents in the load, $\cos\varphi$ the power factor of the load and m the modulation depth used for PWM (amplitude, normalized between 0 and 1, of the reference voltage for sinusoidal PWM[7]). A normalized cartography $RMS\,(I_c)\,/I_{\max}$ as a function of m and φ is shown in Figure 6.3.

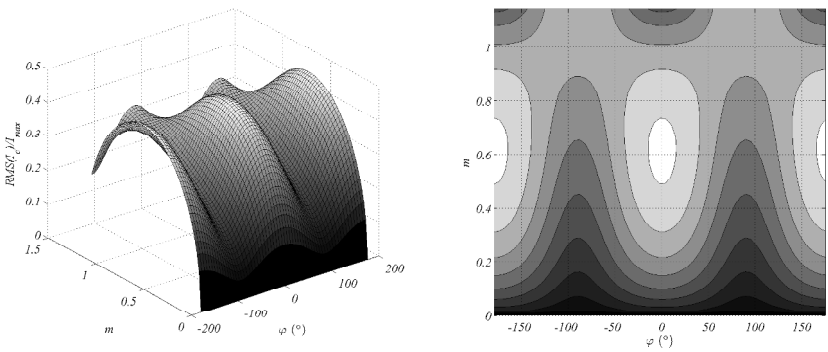


Figure 6.3. *Cartography of $RMS\,(I_c)\,/I_{\max}$ as a function of m and φ for APWM strategies*

7 This definition means that m may be greater than 1 for PWM with zero sequence injection (vector PWM or level 3 harmonic).

This cartography clearly shows the most critical operating points (i.e. the points of highest stress) for a capacitor with a high power factor ($\varphi = 0$) and a modulation depth of the order of 0.6. Assuming (as we are dealing with a normalized characteristic) that the maximum current obtained for a power of $6\,\text{kW}$ (i.e. $13.7\,\text{A}$) can be injected into the load at this operating point, we deduce that:

$$RMS\,(I_c) = I_{\max} \times 0.45 = 6.17\,\text{A} \qquad [6.32]$$

It is therefore important to verify that the capacitor(s) used will withstand this effective current value. If not, the current will need to be distributed across a greater number of elements; in this case, the critical design element is the processed current, rather than the capacitance (this is particularly true for applications with low voltages and high currents, and in the case of electrolytic capacitor technologies).

6.4.5. *Capacitor life expectancy*

The life expectancy of DC link capacitors depends on a number of factors, including:

– the technology used (aluminum or tantalum electrolytic, plastic film, ceramic, etc.);

– the operating voltage compared to the rated voltage of the component;

– the operating current compared to the rated current of the component;

– the ambient temperature.

Temperature is a key element in the aging of capacitors (particularly for aluminum electrolytic capacitors). This element is not only determined by the ambient temperature (which may be high or very high in a vehicle, due to proximity

to a heat engine, for example), but also by self-heating of the component due to Joule losses resulting from their equivalent series resistance (ESR). Aging in a capacitor involves progressive evaporation of the electrolyte, and an increase in the ESR for a given temperature[8].

A formula for calculating the life expectancy D (in hours) is provided in manufacturer documentation issued by Kemet [KEM 12]:

$$D = A.2^{\frac{T_{\text{ref}}-T}{C}} \qquad [6.33]$$

where A and C are the component parameters in hours and in °C respectively. T_{ref} is the reference temperature specified by the manufacturer for a range of components, whilst T is the real operating temperature. We may verify that if $T = T_{\text{ref}}$, the life expectancy will be equal to A.

To take an example, let us consider a capacitance of $50\,\mu$F, calculated above to satisfy the filtering requirements of a component with a rectifier output at $300\,$Hz. Two $100\,\mu$F capacitors from the Kemet ALS30 range, with a nominal voltage of $350\,$V, used in series, will be sufficient. This association corresponds to an equivalent capacitance of $50\,\mu$F supporting $700\,$V; in our application, the DC bus operates at a voltage of $538\,$V (the element is therefore over-dimensioned by around $30\,\%$). However, for this voltage range ($350\,$V), the lowest available capacitance value is $330\,\mu$F, giving an overall capacitance of $165\,\mu$F after integration into a series.

We must then ensure that the capacitors are able to withstand the current circulating through them, i.e.:

– a component at $300\,$Hz with a peak-to-peak amplitude of $558\,$mA (i.e. $0.2\,\text{A}_{\text{RMS}}$.);

8 Note that ESR varies considerably as a function of temperature. From manufacturer documentation, we see that "cold" ESR (@25°C) may be three times higher than that for a nominal temperature (for example 85 or 105°C).

– a component, which we shall assume to be concentrated at the switching frequency, with an effective value of 6.17 A.

The data supplied by the manufacturer concerning these acceptable currents is as follows:

– component at 100 Hz of 2.4 A;

– component at 10 kHz of 5 A.

We note that the capacitor is perfectly suitable with regards to the "low frequency" component, but is *a priori* insufficient to deal with the required HF current. It would therefore be better to use the next capacitor in the range ($470\ \mu$F), which is able to withstand:

– 3.4 A at 100 Hz;

– 7.2 A at 10 kHz.

Finally, we may make use of an on-line tool (www.kemet.com:8080/elc) to evaluate the life expectancy of a capacitor. This tool gives a more precise result than formula [6.33], taking account of the actual operating voltage of the capacitor, and linking the internal temperature of the capacitor to the ambient temperature and to heating (as a function of current) based on a thermal model for the relevant capacitor model (in our case, an ALS30A471DE350 capacitor). The results of this analysis are given in Figure 6.4 and show that, based on our choices, the component has a life expectancy of 165.37 krs (i.e. 18.86 years of constant use). The capacitor is used well below the maximum specifications, with a maximum core temperature of 53.11°C. On the other hand, the maximum authorized temperature is 105°C.

REMARK 6.4.– The Kemet life expectancy calculations are based on doubling of the ESR, and not on full failure of the capacitor (such as a short-circuit or destruction).

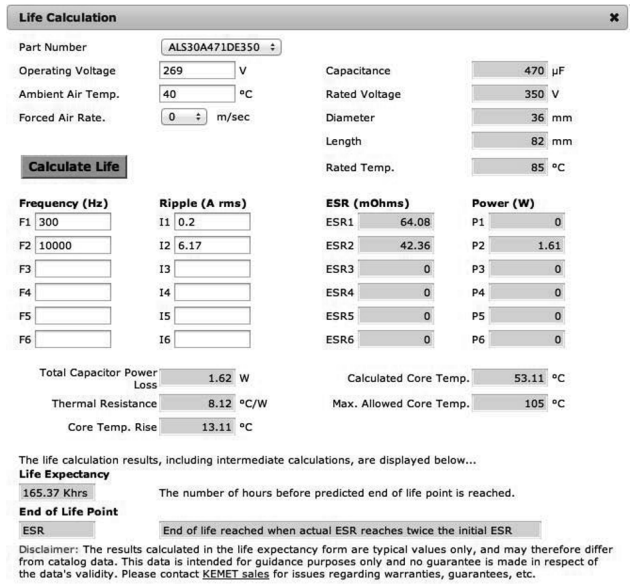


Figure 6.4. *On-line simulation of capacitor life expectancy (source: Kemet)*

6.4.6. *Brake chopper*

For the brake chopper, we need to evaluate the ability of the capacitance to dissipate a power of the order of $6\,\mathrm{kW}$. Braking is generally a transient phenomenon; while the inverter is able to withstand this power value, this is not necessarily the case for the chopper, as in this case the power travels through a single transistor.

We should begin by determining the operating mode of the chopper. Classically, hysteresis control (see Figure 6.5) of the voltage at the capacitor terminals enables robust and simple control. As the nominal voltage U_0 is $538\,\mathrm{V}$, we may fix a chopper switch-on voltage at $U_{\max} = 1.1 \times U_0 = 592\,\mathrm{V}$ (conserving a safety margin greater than 2 with regards to the rated voltage of the components) and a switch-off voltage of $U_{\mathrm{off}} = 1.05 \times U_0 = 565\,\mathrm{V}$. The two hysteresis thresholds

must both be higher than the nominal voltage as, based on the equivalent model of the system presented in Figure 6.6, the bus voltage can never be lower than U_0: calibration at $U_{\text{off}} < U_0$ would mean that the brake chopper would never be switched off once it has been switched on (this is clearly not desirable). The voltage difference between the two thresholds must be sufficient to moderate the switching frequency, and thus to limit switching losses.

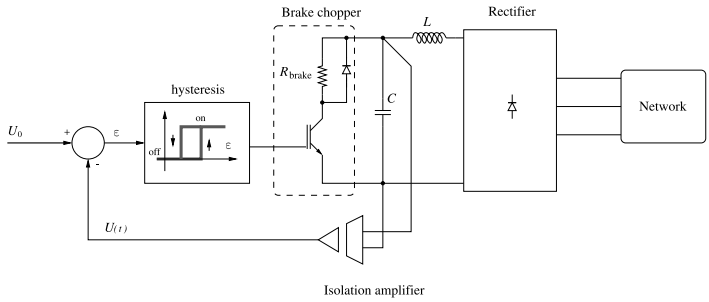


Figure 6.5. *Hysteresis control of the DC bus voltage*

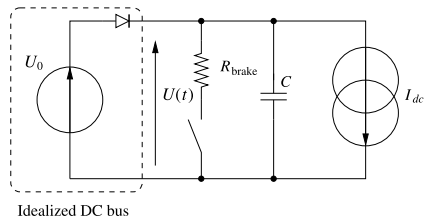


Figure 6.6. *Electrical model of the DC bus and the brake chopper*

REMARK 6.5.– When braking has finished, the voltage does not remain at U_{off} indefinitely, even if the inverter does not return to motor operating mode. Capacitor leaks will lead to discharge until U_0 is reached.

We may thus calculate the average voltage U_{av} during operation of the chopper:

$$U_{\text{av}} = \frac{U_{\max} + U_{\text{off}}}{2} = 578\,\text{V} \qquad [6.34]$$

From this, we may deduce the current I_{brake} which needs to circulate in the brake resistance to ensure dissipation of $P_{\text{brake}} = 6\,\text{kW}$:

$$I_{\text{brake}} = \frac{P_{\text{brake}}}{U_{\text{av}}} = 10.38\,\text{A} \qquad [6.35]$$

We can thus determine the brake resistance. This allows a dissipation of $6\,\text{kW}$ with an average voltage of $578\,\text{V}$, and takes the value:

$$R_{\text{brake}} = \frac{U_{\text{av}}^2}{P_{\text{brake}}} = 55.7\,\Omega \qquad [6.36]$$

Given the model of the brake chopper transistor (which we shall suppose to be identical to that of the inverter transistors[9] – $V_{TO} = 0.75\,\text{V}$ and $R_d^T = 75\,\text{m}\Omega$), we can calculate the conduction losses:

$$P_{\text{cond}}^{\text{brake}} = 15.7\,\text{W} \qquad [6.37]$$

The acceptable loss budget for this transistor is around $55\,\text{W}$. This figure leaves a considerable margin for switching losses. Taking a maximum dissipatable power value of $6\,\text{kW}$, the chopper will not switch, and so there will be no losses of this type. Switching losses will only occur for lower effective braking powers.

Detailed analysis of switching may become complex, as it is highly dependent on the load (mechanical inertia) and on the control technique (e.g. field-oriented control – FOC) used for the "converter/machine" system. However, we may analyze behavior at a particular operating point at

9 NB: the chosen module (SKiiP12AC126V1) only includes a three-phase inverter, and does not contain a brake chopper or a rectifier. However, we shall use the same characteristics for the transistor and diode in the brake chopper as for the components integrated into the inverter (in both electrical and thermal terms).

half-power (i.e. $3\,\text{kW}$). To do this, given the low voltage ripple (between 105 and $110\,\%$ of the nominal voltage), we may assimilate the "converter/machine" assembly to an equivalent current source as $I_{dc} = -\frac{3000[\text{W}]}{578[\text{V}]} = -5.2\,\text{A}$ from the perspective of the DC bus.

Two distinct configurations are possible:

1) "chopper OFF" mode, where the current source I_{dc} charges the capacitor C with voltage U_{off} at voltage $U_{\max}$;

2) "chopper ON" mode, where the current source I_{dc} is connected not only to C, but also toR_{brake}, leading to voltage dropoff.

We therefore need to calculate the operating times in each mode to determine the switching frequency (and the associated losses).

6.4.6.1. *"Chopper OFF" mode*

If the chopper is switched off (open), the system evolves in a configuration where a current source (presumed to be constant) charges a capacitor. Thus:

$$\frac{\Delta U}{T_{OFF}} = -\frac{I_{dc}}{C} \qquad [6.38]$$

where T_{OFF} is the duration of this operating phase, $\Delta U = U_{\max} - U_{\text{off}} = 27\,\text{V}$, $I_{dc} = -5.2\,\text{A}$ and $C = 48.5\,\mu\text{F}$. Hence:

$$T_{OFF} = -\frac{C.\Delta U}{I_{dc}} = 252\,\mu\text{s} \qquad [6.39]$$

6.4.6.2. *"Chopper ON" mode*

If the chopper is closed, we obtain an association in parallel to the current source $-I_{dc}$, with a resistance R_{brake} and a capacitor C. The equation model of this circuit gives us:

$$-R_{\text{brake}}.I_{dc} = U\,(t) + R_{\text{brake}}C\frac{dU\,(t)}{dt} \qquad [6.40]$$

where $U(t)$ is the DC bus voltage. We know that this operating phase begins with an initial condition $U(0) = U_{\max}$.

Introducing a time constant $\tau = R_{\text{brake}}C$, solution $U(t)$ to equation [6.40] may be written in the form:

$$U(t) = -R_{\text{brake}}.I_{dc} + A.\text{e}^{-t/\tau} \qquad [6.41]$$

thus:

$$U\,(0) = -R_{\text{brake}}.I_{dc} + A = U_{\max} \Rightarrow A = U_{\max} + R_{\text{brake}}.I_{dc} \qquad [6.42]$$

We thus obtain the expression of $U(t)$, but we are more interested in the value of time T_{ON} allowing us to reach U_{off}:

$$U(T_{ON}) = -R_{\text{brake}}.I_{dc} + \left(U_{\max} + R_{\text{brake}}.I_{dc}\right).\text{e}^{-T_{ON}/\tau} = U_{\text{off}} \qquad [6.43]$$

From this, we deduce the expression of T_{ON}:

$$T_{ON} = -\tau.\ln\left(\frac{U_{\text{off}} + R_{\text{brake}}.I_{dc}}{U_{\max} + R_{\text{brake}}.I_{dc}}\right) = 253\mu\text{s} \qquad [6.44]$$

6.4.6.3. *Braking summary*

We thus obtain quasi-symmetrical operation (duty ratio $50\,\%$) with a full cycle of $505\,\mu s$. The switching frequency is therefore slightly less than 2 kHz (ten times lower than that used for the inverter)[10].

The conduction losses in this case are equal to $15.7\,\text{W}$ for half of the time period, giving an average power of $7.85\,\text{W}$. However, we need to add in switching losses. To do this, we calculate corrected switch-on and switch-off energies (taking $V_{\text{app}} = 578\,\text{V}$ and $I_{\text{app}} = 10.38\,\text{A}$):

$$E_{ON}^{\text{app}} = \frac{V_{\text{app}}.I_{\text{app}}}{V_{\text{ref}}.I_{\text{ref}}} \cdot E_{ON} = 1.13\,\text{mJ} \qquad [6.45]$$

10 Noise disturbance should therefore be expected during braking periods.

$$E_{OFF}^{\text{app}} = \frac{V_{\text{app}}.I_{\text{app}}}{V_{\text{ref}}.I_{\text{ref}}} \cdot E_{OFF} = 1.27\,\text{mJ} \quad [6.46]$$

In these conditions, we may deduce the switching losses for a frequency $F_d = 2\,\text{kHz}$:

$$P_{\text{com}}^{\text{Brake}} = \left(E_{ON}^{\text{app}} + E_{OFF}^{\text{app}}\right).F_d = 4.8\,\text{W} \quad [6.47]$$

The total losses ($12.7\,\text{W}$) are therefore acceptable for the brake chopper when compared to the reference power value ($55\,\text{W}$ at $22\,\text{A}$) deduced from the nominal operation presented in the documentation for each IGBT.

REMARK 6.6.– A free-wheel diode is used in the brake chopper in order to process the (inevitable) inductive behavior of the dissipation resistance and the associated cables. Loss calculations are generally not required for this component, as it is only used for very brief periods. Moreover, the switching losses have been significantly overestimated; in normal circumstances, only switch-off will be dissipative, as the load does not carry a current during switch-on (even after multiple switching cycles); the load is essentially resistive (and not particularly inductive).

6.5. Losses and thermal aspects

We have shown that the semiconductors in our chosen module (Semikron SKiiP 12AC126V1) are able to permanently withstand a power of $6\,\text{kW}$, intended to occur in transient mode and for a duration limited to $10\,\text{s}$. However, in studying thermal dissipation aspects, we shall carry out dimensioning in permanent mode at $3\,\text{kW}$. This choice is clearly arbitrary, but it allows us to study the behavior of the assembly in transient mode in order to analyze temperature increase phenomena, essentially linked to the thermal capacitance of the heatsink. The heatsink is the largest and, often, the heaviest element in a converter, and is directly

affected by the nominal power of the converter via the total losses in the switches $P_{\text{semi}}^{\text{tot}}$ in this case, as it must be able to exchange these losses with the ambient air in permanent mode, maintaining an acceptable temperature for the chips in the module.

For the purposes of this study, let us suppose that:

– the application requires natural cooling (without fans);

– the imposed maximum junction temperature in the semiconductors is +125°C for transistors;

– the base of the module is thermally equipotential (uniform temperature) and the plastic casing is not involved in dissipation;

– the ambient air may reach a maximum temperature of +40°C without derating of the variable speed drive.

6.5.1. *Summary of losses in the inverter*

We calculated the values of losses in transistors during the module selection phase in order to verify adequacy. However, we did not take account of diode behavior in calculating conduction (or switching) losses. If we look more closely at the behavior of a conducting diode, the (affine) model $V_D(I_D)$ is similar to that of a transistor, but using different parameters:

$$V_D = V_{DO} + R_d^D.I_D \qquad [6.48]$$

where $V_{DO} = 1\,\text{V}$ and $R_d^D = 111\,\text{m}\Omega$ (max. @ 150°C); this should be compared to the transistor parameters ($V_{TO} = 0.8\,\text{V}$ and $R_d^T = 110\,\text{m}\Omega$).

In full-wave calculations, we consider that, at each instant, a transistor conducts through a half-bridge, and so losses are always of the form:

$$P_{\text{cond}}^{\text{IGBT}} = V_{TO}.\langle I\rangle + R_d^T.I_{\text{RMS}}^2 \qquad [6.49]$$

In "PWM" mode, however, a transistor and a diode conduct for $\alpha.T_d$ and $(1-\alpha).T_d$ respectively, or vice versa, according to the sign of the current exiting the half-bridge. We may therefore expect to see a difference between the loss values obtained in "full wave" mode, calculated above, and those obtained taking account of dissociated transistor and diode losses.

REMARK 6.7.– Note that losses are calculated using a unitary power factor in the case of the full wave, in order to guarantee that transistors alone will enter into conduction; even without switching, if there is a lag between the sinusoidal phase current wave and the corresponding phase voltage wave, a diode will begin conducting if the signs of the two quantities are different.

Detailed study of losses using switching is difficult, and it is best to use computer-based methods for evaluation purposes. Semikron has created an on-line tool, known as SEMISEL, for this purpose, which may be used for full dimensioning (including cooling equipment). Table 6.1 shows a comparison (in transient mode @ $6\,$kW) of the results obtained in our earlier calculations and the results produced by the on-line program (the "Transistor" and "Diode" results correspond to one component).

Powers (in Watts)	Simplified calculation	Semikron result
"Transistor" conduction losses	6.79	7.57
"Transistor" switching losses	18.77	19
Total "transistor" losses	25.56	27
"Diode" conduction losses	–	0.71
"Diode" switching losses	–	4.45
Total "diode" losses	–	5.16
Total "inverter" losses	153.36	191

Table 6.1. *Comparison between simplified calculations and results produced using the Semikron program*

REMARK 6.8.– The total "converter" losses are obtained by multiplying the losses in a single transistor and a single diode by six. However, the result produced by the Semikron program presents a slight inconsistency (191 W, instead of 192.96 W, obtained by adding together the individual loss values[11]). This difference is hard to explain, as the program operates as a "gray box". Note, however, that the program is particularly efficient, producing a usable result in around a minute, compared to the fifteen minutes required to extract the necessary information from the relevant documentation and carry out highly approximative calculations. This approximation is highly satisfactory (with a difference of 5.3 % compared to the Semikron result for transistor losses) and is entirely suitable for use in the design process. Care should be taken, however, as successful application to a specific example is not proof of systematic validity.

6.5.2. *Summary of losses in the brake chopper*

Losses in the brake chopper have been evaluated with a reasonably high degree of precision in two particular contexts:

– continuous operation (not in switch mode) at full power (6 kW), with losses evaluated as 15.7 W;

– switch-mode operation (2 kHz)at half power (3 kW) with losses evaluated as 7.85 W (conduction) + 4.8 W (switching), giving a total of 12.7 W.

REMARK 6.9.– In this case, losses are located in the transistor alone; in an ideal situation, the powered load (dissipation resistance) is purely resistive, and will only present weak internal (and cabling) inductance. In these conditions, losses in the free wheel diode are negligible. Note,

11 There is even a degree of incoherence between the total losses in a transistor and the sum of conduction and switching losses.

moreover, that for the two operating points, losses remain effectively constant, and we shall therefore use a value of $20\,\mathrm{W}$ systematic losses in the braking chopper (on the condition that the element is working correctly!).

6.5.3. *Calculation of losses in the rectifier*

Finally, we need to evaluate losses in the rectifier. To do this, we note that the diodes are crossed by a continuous current (a good approximation is obtained by applying $10\,\%$ smoothing to the rectifier output current). The DC bus voltage is $538\,\mathrm{V}$ in nominal operating mode, so we can calculate the average current supplied by the rectifier at 3 and $6\,\mathrm{kW}$:

$$\begin{cases} \langle I_{rec} \rangle_{P=3\mathrm{kW}} = 5.58\mathrm{A} \\ \langle I_{rec} \rangle_{P=6\mathrm{kW}} = 11.2\mathrm{A} \end{cases} \qquad [6.50]$$

Let us consider the parameters of the rectifier diodes ($V_{DO} = 0.8\,\mathrm{V}$ and $R_d^D = 34\,\mathrm{m\Omega}$ at 125°C), which, like the brake chopper, are not dependent on the chosen inverter (i.e. the components are not included in the same device). We obtain a direct voltage drop V_F of $990\,\mathrm{mV}$ at $3\,\mathrm{kW}$ and $1.18\,\mathrm{V}$ at $6\,\mathrm{kW}$.

As two diodes are permanently in conduction in a full-wave bridge (PDn, where n is any given value), we may directly write the expression of losses $P_{\mathrm{cap}}^{\mathrm{rec}}$:

$$P_{\mathrm{cap}}^{\mathrm{rec}} = 2V_F . \langle I_{rec} \rangle \qquad [6.51]$$

i.e. $11\,\mathrm{W}$ at $3\,\mathrm{kW}$ and $26.3\,\mathrm{W}$at $6\,\mathrm{kW}$.

Considering losses per individual diode, we obtain values of $1.84\,\mathrm{W}$ and $4.39\,\mathrm{W}$ for the two operating points.

6.5.4. *Summary of losses*

We can now provide an overall vision of losses in the converter, as shown in Table 6.2, using Semikron program data for the inverter.

Powers (in Watts)	@ $3\,kW$	@ $6\,kW$
Total "Inverter Transistor" losses	12	27
Total "Inverter Diode" losses	3.07	5.16
Total "Brake Transistor" losses	12.7	15.7
Total "Rectifier Diode" losses	1.84	4.39
Total "Variable speed drive" losses	114.2	235

Table 6.2. *Summary of total losses*

REMARK 6.10.– The total losses shown for the variable speed drive include those associated with the brake chopper. In motor mode, the brake transistor losses should be subtracted from the total. Note that in "motor" mode, the converter efficiency is $96.7\,\%$ at 3 kW and $96.5\,\%$ at 6 kW, presuming that these reference values are possible variator output powers (3 and $6\,$kW supply to the load, respectively).

6.5.5. *Thermal model and heatsinks*

This detailed study of the distribution of losses between different components in the module allows us to calculate the junction temperatures of individual elements. Clearly, this depends on the level of precision used in the technical documentation, which should specify the thermal resistances linking the chips to the metal base of the casing. In our case, the documentation provides us with the following values:

– thermal resistance of an inverter transistor: $1.3\,$K/W;

– thermal resistance of an inverter diode: $1.92\,$K/W;

– thermal resistance of a chopper transistor: $1.3\,$K/W ;

– thermal resistance of a rectifier diode: $1.5\,$K/W.

These resistances apply to the junction between the semiconductor chip and the heatsink. The latter, requires strong contact (using thermal grease) and correct attachment of the module to the heatsink (torque of between 2 and 2.5 Nm, specified in the documentation).

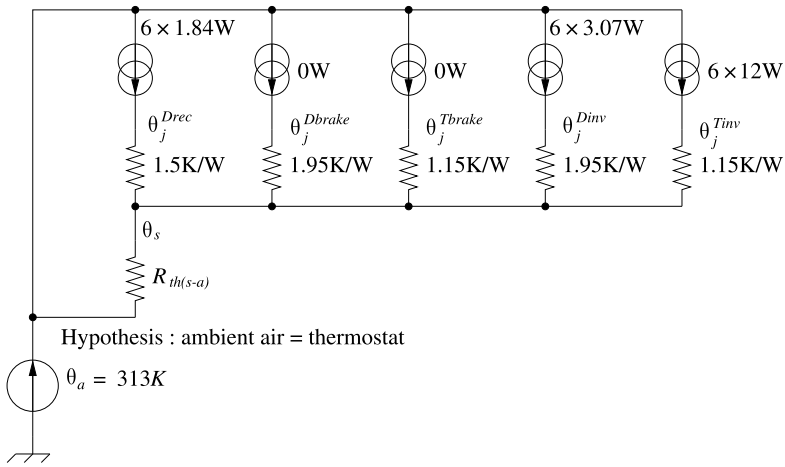


Figure 6.7. *Thermal (electrical) diagram of the inverter*

Based on this information, we can establish a thermal diagram ("electrical" equivalent), shown in Figure 6.7 which includes the resistance $R_{th(s-a)}$ of the heatsink under consideration. We can then express our problem in equations, linking the junction temperatures of the different components to the thermal resistance of the heatsink. This allows us to identify a critical component (generally the transistors in the inverter, as they dissipate considerably more power than the other components) and to determine a value for $R_{th(s-a)}$ based on the maximum acceptable temperature for the component. In this specific case, a node (θ_s) appears, traversed by a heat flux P_{tot} of 101.5 W, originating in all of the components. The temperature in the heatsink is therefore:

$$\theta_s = \theta_a + R_{th(s-a)}.P_{\text{tot}} \qquad [6.52]$$

The evaluation of the junction temperature of a transistor in the inverter gives us:

$$\begin{aligned}\theta_j^{Tinv} &= \theta_s + 1.15 \times 12 = 313 + R_{th(s-a)} \times 101.5 + 1.15 \times 12 \\ &\simeq R_{th(s-a)} \times 101.5 + 326.8\end{aligned} \quad [6.53]$$

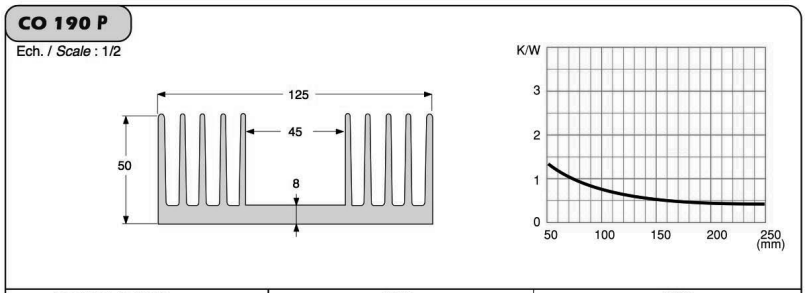
If we impose a maximum junction temperature of 125°C (398 K) for the transistors, a heatsink with a thermal resistance of 0.702 K/W is required. In these conditions, the heatsink temperature is equal to 111°C (protection should therefore be put in place to avoid direct contact with users, or users should be made aware that the element becomes hot during use).

Clearly, we need to ensure that the selected heatsink model (profile shown in Figure 6.8 over a length of 110 mm) is compatible with the packaging of the component (or model) requiring cooling. In this case, the base of the module (41.6 mm x 39.5 mm) has a central M4 threaded screw, which can easily be placed on the flange-free side of the heatsink, as in the case of the rectifier and the brake chopper. A rectifier may also be placed in this area. Moreover, we need to ensure that the heatsink is used with the flanges oriented vertically in order to maximize cooling efficiency in cases where fans are not used to force air to circulate.

6.5.6. *Transient study*

We may now consider the behavior of the "variable speed drive + heatsink" assembly for a transient period at 6 kW in order to determine whether this transition will induce an unacceptable temperature increase. In our specific case, the junction temperature for the transistors in the inverter in permanent mode is set at 125°C. Manufacturer documentation for the module states that the element may be

used with no risk of damage[12] at temperatures of up to 150°C. This leaves us a margin of 25°C for the transient mode.



Longueur / *Length*	1000	1000
Usinage / *Layout*	-	-
Finition / *Finish*	Brut /*Raw*	Anodisé Noir /*Black anodized*
CODE	**31019010**	**31019013**

Figure 6.8. *Extract from manufacturer documentation for a range of heatsinks (source: SEEM)*

We therefore need to consider the thermal dynamics of the temperature in this case, and to do this, we must analyze the thermal capacitance(s) present in the system. For the purposes of our model, we shall only consider the heatsink, which is the element with the highest mass, and thus the element with the greatest thermal inertia. We need to know the material used (aluminum) in order to obtain the specific heat value (897 J/kg/K) and the mass of the heatsink. The linear density of the profile is not specified in the documentation, and we need to calculate the mass of the heatsink by calculating its volume and multiplying this value by the density of aluminum (2 700 kg/m^3). Unfortunately, we only obtain an approximate value, as the rating of the profile is incomplete with regards to the flanges (in this case, we shall presume that the flanges have a thickness of 3 mm). We shall also use a profile length of 110 mm for our calculations.

12 With the exception of accelerated aging

We thus obtain the following volume $\mathcal{V}$:

$$\mathcal{V}\left[\mathrm{mm}^3\right] = \underbrace{8 \times 125 \times 110}_{\text{volume of plate}} + 10 \times \underbrace{3 \times 42 \times 110}_{\text{volume of flange}} = 248\,600 \qquad [6.54]$$

This volume of $248.6 \times 10^{-6}\,\mathrm{m}^3$ gives us a mass of $671\,\mathrm{g}$ for the heatsink, and therefore a thermal capacitance $C_{th(s-a)}$ of $602\,\mathrm{J/K}$. We can thus modify the thermal model by placing this thermal capacitance in parallel to $R_{th(s-a)}$.

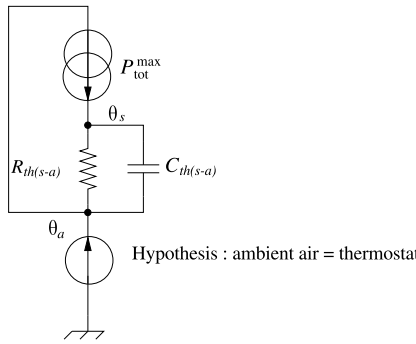


Figure 6.9. *Simplified transient thermal diagram*

For the purposes of this transient study, it is simpler to combine all of the power sources initially (see Figure 6.9) to evaluate the heatsink temperature, then to calculate the junction temperatures of the different components *a posteriori*. The selected operating point corresponds to the critical case, with a power of $6\,\mathrm{kW}$ in braking mode and total losses $P_{\mathrm{tot}}^{\max}$ of $189.6\,\mathrm{W}$. The equation model of the equivalent system, taking $\Delta\theta = \theta_s - \theta_a$, gives us:

$$P_{\mathrm{tot}}^{\max} = \frac{\Delta\theta}{R_{th(s-a)}} + C_{th(s-a)} \cdot \frac{d\Delta\theta}{dt} \qquad [6.55]$$

The solution to this differential gives us (taking $\tau_{th(s-a)} = R_{th(s-a)}.C_{th(s-a)}$):

$$\Delta\theta\,(t) = R_{th(s-a)}.P_{\mathrm{tot}}^{\max} + A.\mathrm{e}^{-t/\tau_{th(s-a)}} \qquad [6.56]$$

where A is dependent on the initial conditions. In the least favorable case, we need to consider that this transient period does not start from cold, but following prolonged operation in permanent mode (with a heatsink at 111°C and an ambient temperature of 40°C – i.e. $\Delta\theta(0) = 71$°C). We therefore take:

$$A = \Delta\theta\,(0) - R_{th(s-a)}.P_{\text{tot}}^{\max} \simeq -82,7\text{°C} \qquad [6.57]$$

We can then evaluate the evolution of $\Delta\theta$ after $10\,\text{s}$ of operation in this mode:

$$\Delta\theta\,(10\text{s}) = 72.9\text{°C} \qquad [6.58]$$

This shows that transient operation at $6\,\text{kW}$ for a period of $10\,\text{s}$ only produces an increase of 1.9°C in the heatsink, thanks to the thermal time constant of the element ($\tau_{th(s-a)} = 422.6\,\text{s}$). We may then consider the temperatures of the different components included in the heatsink, to check that none of these elements exceeds a critical threshold. If these thresholds are not respected, the heatsink will need to be modified, or a different cooling technology may be used (see Volume 1 [PAT 15a], Chapter 3).

Appendix 1

Formulas for Electrical Engineering and Electromagnetism

A1.1. Sinusoidal quantities

A1.1.1. *Scalar signals*

A1.1.1.1. *Definitions*

Sinusoidal waveforms are extremely widespread in electrical engineering, both for voltages and for currents. In this case, we will consider a generic signal of the form:

$$x(t) = X_{\max} \cos(\omega t - \varphi) \qquad [A1.1]$$

This real signal is associated with an equivalent complex signal:

$$\underline{x}(t) = X_{\max}.\mathrm{e}^{j(\omega t - \varphi)} \qquad [A1.2]$$

This vector may be represented in the complex plane. We obtain a circular trajectory of radius $X_{\max}$ with a vector rotating at a constant speed ω in a counterclockwise direction. This representation (which is widespread in electrical engineering) is known as a Fresnel diagram (or, more simply, a vector diagram).

REMARK A1.1.– Derivation and integration calculations are greatly simplified in the complex plane, as they are replaced, respectively, by multiplying or dividing by $j\omega$. To return to the real domain, we simply take the real part of the corresponding complex signal: $x(t) = \mathfrak{Re}\left[\underline{x}\left(t\right)\right]$.

The rotating component $\mathrm{e}^{j\omega t}$ of the complex vectors is meaningless when studying linear circuits; the *amplitudes* and the relative phases between the different quantities under study are the only important elements. Note that an absolute phase for a sinusoidal value would be meaningless; the choice of a reference value of the form $X_{\mathrm{ref}}.\cos(\omega.t)$, associated with the vector $X_{\mathrm{ref}}.\mathrm{e}^{j\omega t}$, is purely arbitrary.

Complex vectors are also often represented (in the literature) using the RMS value of the real value in question as the modulus, and not the real amplitude.

A1.1.1.2. *Trigonometric formulas*

When making calculations using complex values, we need Euler's formulas:

$$\begin{cases} \cos\theta = \frac{\mathrm{e}^{j\theta}+\mathrm{e}^{-j\theta}}{2} \\ \sin\theta = \frac{\mathrm{e}^{j\theta}-\mathrm{e}^{-j\theta}}{2j} \end{cases} \qquad \text{[A1.3]}$$

These two formulas can be used to give the four basic trigonometric formulas used in electrical engineering:

$$\begin{cases} \cos\left(a+b\right) = \cos a\cos b - \sin a\sin b \\ \cos\left(a-b\right) = \cos a\cos b + \sin a\sin b \\ \sin\left(a+b\right) = \sin a\cos b + \cos a\sin b \\ \sin\left(a-b\right) = \sin a\cos b - \cos a\sin b \end{cases} \qquad \text{[A1.4]}$$

These four equations allow us to establish four further equations:

$$\cos a\cos b = \frac{1}{2}\left(\cos\left(a+b\right) + \cos\left(a-b\right)\right) \qquad \text{[A1.5]}$$

$$\begin{cases} \cos a \cos b = \frac{1}{2}\left(\cos\left(a+b\right) + \cos\left(a-b\right)\right) \\ \sin a \sin b = \frac{1}{2}\left(\cos\left(a-b\right) - \cos\left(a-b\right)\right) \\ \sin a \cos b = \frac{1}{2}\left(\sin\left(a+b\right) + \sin\left(a-b\right)\right) \\ \cos a \sin b = \frac{1}{2}\left(\sin\left(a+b\right) - \sin\left(a-b\right)\right) \end{cases} \quad [A1.6]$$

A1.1.2. *Vector signals (three-phase context)*

A1.1.2.1. *Reference frame* (a, b, c)

Three-phase systems are very much common in electrical engineering, particularly balanced three-phase systems. A vector $(\mathbf{x}_3) = (x_a, x_b, x_c)^t$ with three balanced components is therefore expressed as:

$$(\mathbf{x}_3) = X_{\max} \begin{pmatrix} \cos\theta \\ \cos\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) \end{pmatrix} \text{ where } \theta = \omega.t + \phi_0 \quad [A1.7]$$

in the case of a direct system, or:

$$(\mathbf{x}_3) = X_{\max} \begin{pmatrix} \cos\theta \\ \cos\left(\theta + \frac{2\pi}{3}\right) \\ \cos\left(\theta - \frac{2\pi}{3}\right) \end{pmatrix} \text{ where } \theta = \omega.t + \phi_0 \quad [A1.8]$$

in the inverse case.

DEFINITION A1.1.– A balanced three-phase system is thus made up of three sinusoids of the same amplitude and same frequency, with a phase deviation of $\frac{2\pi}{3}$.

A direct three-phase system is characterized by the fact that, taking phase 1 as a reference point (i.e. first component), the second component has a delay of 120° (in a balanced situation) and the third component presents a delay of 120° in relation to the second component.

An inverse three-phase system is characterized by the fact that, taking phase 1 as a reference point (i.e. first

component), the third component has a delay of 120° (in a balanced situation) and the second component presents a delay of 120° in relation to the third component. A direct system can be converted into an inverse system (and vice versa) by permutations of two components.

A1.1.2.2. *Three-phase to two-phase transformation* (α, β)

It is important to note that a balanced three-phase system (whether direct or inverse) presents an important property in that the sum of the components is null:

$$x_a + x_b + x_c = 0 \qquad \text{[A1.9]}$$

This sum is classically referred to as the zero sequence component (denoted as x_0). A balanced three-phase system is therefore not linearly independent in that, given two of the components, we may calculate the value of the third component. It is therefore possible to propose a three-phase to two-phase transformation without any information loss. The simplest transformation, known as the Clarke (abc-to-$\alpha\beta$) transformation, allows us to associate an initial vector $(\mathbf{x}_3) = (x_a, x_b, x_c)^t$ with an equivalent two-phase vector $(\mathbf{x}_{\alpha\beta}) = (\mathbf{x}_2) = (x_\alpha, x_\beta)^t$ using components of the same amplitude as those in the initial vector. This operation introduces the Clarke matrix C_{32}:

$$X_{\max}\begin{pmatrix}\cos\theta\\ \cos\left(\theta+\frac{2\pi}{3}\right)\\ \cos\left(\theta-\frac{2\pi}{3}\right)\end{pmatrix} = X_{\max}.\underbrace{\begin{pmatrix}1 & 0\\ -1/2 & \sqrt{3}/2\\ -1/2 & -\sqrt{3}/2\end{pmatrix}}_{C_{32}}.\begin{pmatrix}\cos\theta\\ \sin\theta\end{pmatrix} \qquad \text{[A1.10]}$$

This gives the following direct transformation:

$$(\mathbf{x}_3) \triangleq C_{32}.(\mathbf{x}_2) \qquad \text{[A1.11]}$$

The Clarke transformation may be extended by taking account of the zero sequence component x_0, presented in [A1.9]:

$$(\mathbf{x}_3) \triangleq C_{32}.(\mathbf{x}_2) + C_{31}.x_0 \qquad \text{[A1.12]}$$

with:

$$C_{31} = \begin{pmatrix} 1 \\ 1 \\ 1 \end{pmatrix} \qquad \text{[A1.13]}$$

Noting certain properties of matrices C_{32} and C_{31}:

$$\begin{aligned} C_{32}^t C_{32} &= \tfrac{3}{2}\begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \;;\; C_{31}^t C_{31} = 3 \\ C_{32}^t C_{31} &= \begin{pmatrix} 0 \\ 0 \end{pmatrix} \;;\; C_{31}^t C_{32} = \begin{pmatrix} 0 & 0 \end{pmatrix} \end{aligned} \qquad \text{[A1.14]}$$

we can establish the inverse transformation:

$$(\mathbf{x}_2) \triangleq \frac{2}{3} C_{32}^t.(\mathbf{x}_3) \qquad \text{[A1.15]}$$

and:

$$x_0 \triangleq \frac{1}{3} C_{31}^t.(\mathbf{x}_3) \qquad \text{[A1.16]}$$

A1.1.2.3. *Concordia variant*

A second three-phase to two-phase transformation is also widely used in the literature, with properties similar to those of the Clarke transformation. This variation does not retain the amplitudes of the transformed values, but allows us to retain powers. This operation is known as the Concordia transformation and is based on two matrices, denoted T_{32} and T_{31}, deduced from C_{32} and C_{31}:

$$T_{32} = \sqrt{\frac{2}{3}} C_{32} \;;\; T_{31} = \frac{1}{\sqrt{3}} C_{31} \qquad \text{[A1.17]}$$

The properties of these matrices are deduced from those established in [A1.14]:

$$\begin{aligned} T_{32}^t T_{32} &= \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} \; ; \; T_{31}^t T_{31} = 1 \\ T_{32}^t T_{31} &= \begin{pmatrix} 0 \\ 0 \end{pmatrix} \; ; \; T_{31}^t T_{32} = \begin{pmatrix} 0 & 0 \end{pmatrix} \end{aligned} \qquad \text{[A1.18]}$$

This produces a direct transformation of the form:

$$(\mathbf{x}_3) \triangleq T_{32}.(\mathbf{x}_2) + T_{31}.x_0 \qquad \text{[A1.19]}$$

with the following inverse transformation:

$$(\mathbf{x}_2) \triangleq T_{32}^t.(\mathbf{x}_3) \qquad \text{[A1.20]}$$

and:

$$x_0 \triangleq T_{31}^t.(\mathbf{x}_3) \qquad \text{[A1.21]}$$

A1.1.2.4. *Park transformation*

The Park (abc-to-dq) transformation consists of associating the Clarke (or Concordia) transformation with a rotation in the two-phase reference plane (α, β) onto a reference frame (d, q). This operation is carried out using the rotation matrix $P(\theta)$, defined as:

$$P(\theta) = \begin{pmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{pmatrix} \qquad \text{[A1.22]}$$

Thus, if we associate a vector $(\mathbf{x}_{dq}) = (x_d, x_q)^t$ with the initial two-phase vector $(\mathbf{x}_{\alpha\beta}) = (\mathbf{x}_2)$ (obtained from a Clarke or Concordia transformation), we obtain the following relationship:

$$(\mathbf{x}_{\alpha\beta}) = (\mathbf{x}_2) \triangleq P(\theta).(\mathbf{x}_{dq}) \qquad \text{[A1.23]}$$

The choice of a frame of reference involves the definition of angle θ, selected arbitrarily. Generally, the chosen reference frame is synchronous with the rotating values (sinusoidal components with an angular frequency ω), but this is not obligatory.

The following (non-exhaustive) list shows a number of properties of matrix $P(\theta)$:

$$P(0) = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix} = \mathbb{I}_2 \; ; \; P\left(\tfrac{\pi}{2}\right) = \begin{pmatrix} 0 & -1 \\ 1 & 0 \end{pmatrix} = \mathbb{J}_2 \text{ such that } \mathbb{J}_2 = -\mathbb{I}_2 \quad \text{[A1.24]}$$

$$P(\alpha+\beta) = P(\beta+\alpha) = P(\alpha).P(\beta) = P(\beta).P(\alpha) \quad \text{[A1.25]}$$

$$P(\alpha)^{-1} = P(\alpha)^t = P(-\alpha) \quad \text{[A1.26]}$$

$$\frac{d}{dt}[P(\alpha)] = \frac{d\alpha}{dt} \cdot P\left(\alpha + \tfrac{\pi}{2}\right) = \frac{d\alpha}{dt} \cdot P(\alpha) \cdot P\left(\tfrac{\pi}{2}\right) = \mathbb{J}_2 \frac{d\alpha}{dt} \cdot P(\alpha) \quad \text{[A1.27]}$$

A1.1.2.5. *Phasers or complex vectors*

The matrix formalism of the Clarke, Concordia and Park transformations may be replaced by an equivalent complex representation. Evidently, a rotation of the frame of reference by angle θ may be obtained by using a complex coefficient $\mathrm{e}^{j\theta}$ as easily as with a rotation matrix $P(\theta)$. To this end, we use a "phaser" $\underline{x}_s$ defined in a stationary frame of reference:

$$\underline{x}_s = x_\alpha + j.x_\beta \quad \text{[A1.28]}$$

The phaser is also defined in a rotating frame ($\underline{x}_r$):

$$\underline{x}_r = x_d + j.x_q \quad \text{[A1.29]}$$

Note that these complex representations may be obtained using matrix transformations. The real transformations seen in the previous sections each have an equivalent complex transformation, as shown in Table A1.1.

Real transformation	Complex transformation
Clarke	Fortescue
Concordia	Lyon
Park	Ku

Table A1.1. *Correspondence between real and complex transformations (names)*

A1.2. General characteristics of signals in electrical engineering

This section presents the formulas used for calculating the *general characteristics of periodic signals* traditionally encountered in electrical engineering. However, it does not cover formulas related to spectral analysis, which are covered in Appendix 2 of this Volume and Volume 4 [PAT 15c].

In this section, we will therefore cover the formulas used to calculate the average and RMS values of given quantities, applied to two widespread signal types: sinusoids and the asymmetric square signal of duty ratio α.

A1.2.1. *Average value*

A1.2.1.1. *General definition*

The average value $\langle x \rangle$ of a T-periodic signal $x(t)$ is defined generally by the integral:

$$\langle x \rangle = \frac{1}{T} \int_0^T x(t).dt \qquad \text{[A1.30]}$$

REMARK A1.2.– In this case, the integration limits are chosen arbitrarily. Only the interval between the two limits is important, and it must be equal to T.

A1.2.1.2. *Sinusoids*

In the case of sinusoids, we evidently obtain an average value of zero.

A1.2.1.3. *Asymmetric square*

The T-periodic asymmetric square $x(t)$ studied here has a certain value X_0 during a period αT, then 0 for the rest of the period. We can therefore write the average value $\langle x \rangle$ directly:

$$\langle x \rangle = \frac{1}{T} \int_0^T x(t).dt = \frac{1}{T} \int_0^{\alpha T} X_0.dt = \alpha.X_0 \qquad \text{[A1.31]}$$

A1.2.2. *RMS value*

A1.2.2.1. *General definition*

The RMS value X_{rms} of a T-periodic signal $x(t)$ is defined generally by the integral:

$$X_{\text{rms}} = \sqrt{\frac{1}{T} \int_0^T x^2(t).dt} \qquad \text{[A1.32]}$$

REMARK A1.3.– When calculating the average value, the integration limits are chosen arbitrarily. Only the interval between the two limits is important, and it must be equal to T.

A1.2.2.2. *Sinusoids*

For a sinusoid of amplitude X_{max}, the RMS value is $X_{\text{rms}} = \frac{X_{\text{max}}}{\sqrt{2}}$.

A1.2.2.3. *Asymmetric square*

The T-periodic asymmetric square $x(t)$ defined in section A1.2.1 presents an RMS value expressed as:

$$X_{\text{rms}} = \sqrt{\frac{1}{T} \int_0^{\alpha T} X_0^2.dt} = \sqrt{\alpha}.X_0 \qquad \text{[A1.33]}$$

A1.3. Energy and power

A1.3.1. *Energy*

In mechanics, energy is obtained by the operation of a force over a certain distance. In electrical engineering, this term corresponds to the movement of a charge following a variation in electrical potential. In particle physics, a unit known as an electron-volt (eV) is used for energy values at the atomic level. The energy formulas used in power electronics (expressed in Joules (J)) correspond to the energy stored in an inductance or a capacitor.

In an inductance, the energy E_L (magnetic energy) depends on the current I and the inductance L:

$$E_L = \frac{1}{2} L I^2 \qquad \text{[A1.34]}$$

For a capacitor, the energy E_C (electrostatic energy) depends on the voltage V and the capacitance C:

$$E_C = \frac{1}{2} C V^2 \qquad \text{[A1.35]}$$

A1.3.2. *Instantaneous power*

The instantaneous power $p(t)$ given – or provided to – the dipole is linked, according to the passive sign convention (PSC), to the voltage $v(t)$ at its terminals and the current $i(t)$ passing through it as follows:

$$p(t) = v(t).i(t) \qquad \text{[A1.36]}$$

This power is defined in watts (W). It is linked to the energy consumed E (in J) between two instants t_1 and t_2 by the following integral:

$$E = \int_{t_1}^{t_2} p(t).dt \qquad \text{[A1.37]}$$

The instantaneous power $p(t)$ is connected to the variation in energy $e(t)$ which can also be defined (up to an additive constant) as a function of time. In this case, we obtain:

$$p\,(t) = \frac{de\,(t)}{dt} \qquad \text{[A1.38]}$$

A1.3.3. *Average power*

As for any T-periodic signal, the average power P is obtained using the following formula:

$$P = \frac{1}{T}\int_0^T p(t).dt = \frac{1}{T}\int_0^T v(t).i(t).dt \qquad \text{[A1.39]}$$

In the case of a resistive charge R, we can establish the following relationship (Ohm's law):

$$v(t) = R.i(t) \qquad \text{[A1.40]}$$

This allows us to formulate two possible expressions for this power:

$$P = \frac{R}{T}\int_0^T i^2(t).dt = R.I_{\text{rms}}^2 \qquad \text{[A1.41]}$$

and:

$$P = \frac{1}{RT}\int_0^T v^2(t).dt = \frac{V_{\text{rms}}^2}{R} \qquad \text{[A1.42]}$$

where V_{rms} and I_{rms} are the RMS values of the voltage and the current, respectively.

A1.3.4. *Sinusoidal mode*

A1.3.4.1. *Single phase*

In single phase sinusoidal operating mode, we can, generally speaking, consider a voltage $v(t)$ of the form:

$$v(t) = V_{\text{rms}}\sqrt{2}\cos(\omega t) \qquad \text{[A1.43]}$$

as the phase reference, with a current, with a phase deviation angle φ (the lag in relation to the voltage), expressed as:

$$i(t) = I_{\text{rms}}\sqrt{2}\cos(\omega t - \varphi) \qquad \text{[A1.44]}$$

Calculating the instantaneous power obtained using these two values, we obtain:

$$p(t) = V_{\text{rms}}I_{\text{rms}}(\cos(2\omega t - \varphi) + \cos\varphi) \qquad \text{[A1.45]}$$

We thus obtain two terms:

– a constant term, which is, evidently, the average power, referred to in this context as active power;

– a variable term, with an angular frequency of 2ω, known as fluctuating power.

The first interesting result is, therefore, the expression of the average (active) power P:

$$P = V_{\text{rms}}I_{\text{rms}}\cos\varphi \qquad \text{[A1.46]}$$

In terms of voltage dimensioning (thickness of insulation) and current dimensioning (cross-section of conductors) of equipment, the real power value used for design purposes is known as the apparent power S , and is obtained by directly multiplying the RMS voltage value by the RMS current value:

$$S = V_{\text{rms}}I_{\text{rms}} \qquad \text{[A1.47]}$$

To emphasize the "fictional" character of this power, it is not given in W, but in volt-amperes (VA).

In electrical engineering, we then use the notion of *reactive power* Q, which allows us to establish a connection between the active power P and the apparent power S. This is expressed as:

$$Q = V_{\text{rms}} I_{\text{rms}} \sin \varphi \qquad \text{[A1.48]}$$

The connection between P, Q and S is thus:

$$S^2 = P^2 + Q^2 \qquad \text{[A1.49]}$$

As in the case of apparent power, this power value is fictional; it is not measured in W, or in VA, but rather in volt ampere reactive (VAR).

REMARK A1.4.– Equation [A1.49] is only valid if the voltage *and* the current are sinusoidal. In non-sinusoidal mode, we introduce an additional power, denoted D, known as the deformed power. This is used to establish a new equation as follows:

$$S^2 = P^2 + Q^2 + D^2 \qquad \text{[A1.50]}$$

The instantaneous power is always positive (respectively, negative) when $\varphi = 0°$ (respectively, $\varphi = 180°$), but if φ takes a different value, $p(t)$ cancels out, changing the sign. In these conditions, the direction of transfer of electronic energy between the source and the load is reversed.

A1.3.4.2. *Three phase*

In a three-phase context, using the "voltage" vector $(\mathbf{v}_3)$ as a point of reference, and more specifically as the first

component, we take (based on the hypothesis of a direct balanced system):

$$(\mathbf{v}_3) = V_{\text{rms}}\sqrt{2}\begin{pmatrix}\cos(\omega t)\\ \cos\left(\omega t - \frac{2\pi}{3}\right)\\ \cos\left(\omega t + \frac{2\pi}{3}\right)\end{pmatrix} \quad \text{[A1.51]}$$

From this, we deduce the "current" vector $(\mathbf{i}_3)$, with a lag in each component when compared to the corresponding components in $(\mathbf{v}_3)$:

$$(\mathbf{i}_3) = I_{\text{rms}}\sqrt{2}\begin{pmatrix}\cos(\omega t - \varphi)\\ \cos\left(\omega t - \frac{2\pi}{3} - \varphi\right)\\ \cos\left(\omega t + \frac{2\pi}{3} - \varphi\right)\end{pmatrix} \quad \text{[A1.52]}$$

A matrix formalism may be used to obtain the expression of the instantaneous power $p(t)$:

$$p(t) = (\mathbf{v}_3)^t \,.\, (\mathbf{i}_3) \quad \text{[A1.53]}$$

In this case, the Park factorization of the "voltage and current" vectors is particularly effective:

$$\begin{aligned}(\mathbf{v}_3) &= V_{\text{rms}}\sqrt{2}.C_{32}\begin{pmatrix}\cos(\omega t)\\ \sin(\omega t)\end{pmatrix}\\ &= V_{\text{rms}}\sqrt{2}.C_{32}.P(\omega t)\,.\begin{pmatrix}1\\0\end{pmatrix}\end{aligned} \quad \text{[A1.54]}$$

$$\begin{aligned}(\mathbf{i}_3) &= I_{\text{rms}}\sqrt{2}.C_{32}\begin{pmatrix}\cos(\omega t - \varphi)\\ \sin(\omega t - \varphi)\end{pmatrix}\\ &= I_{\text{rms}}\sqrt{2}.C_{32}.P(\omega t - \varphi)\,.\begin{pmatrix}1\\0\end{pmatrix}\end{aligned} \quad \text{[A1.55]}$$

Hence:

$$p(t) = 2V_{\text{rms}}.I_{\text{rms}} \begin{pmatrix} 1 & 0 \end{pmatrix} .P\left(-\omega t\right) .C_{32}^{t}.C_{32}.P\left(\omega t - \varphi\right) . \begin{pmatrix} 1 \\ 0 \end{pmatrix} \quad \text{[A1.56]}$$

After simplification, this gives us:

$$p(t) = 3V_{\text{rms}}.I_{\text{rms}} \cos\varphi \quad \text{[A1.57]}$$

Note that we obtain the instantaneous power, and not an average value. This highlights a notable property of three-phase systems: there is no globally fluctuating power in this configuration.

The active power P is therefore defined as follows:

$$P = p(t) = 3V_{\text{rms}}.I_{\text{rms}} \cos\varphi \quad \text{[A1.58]}$$

The notions of reactive power Q and apparent power S are also used in three-phase contexts, with the following expressions:

$$\begin{cases} Q = 3V_{\text{rms}}.I_{\text{rms}} \sin\varphi \\ S = 3V_{\text{rms}}.I_{\text{rms}} \end{cases} \quad \text{[A1.59]}$$

Relationship [A1.49] is therefore still valid in a three-phase context:

$$S^2 = P^2 + Q^2 \quad \text{[A1.60]}$$

Note that variants exist, notably where the notion of line-to-line voltage is used. Voltage V_{rms} is the RMS *line-to-neutral voltage* (i.e. between the phase and the neutral); the neutral is not always accessible, so the notion of line-to-line voltage is often preferred , with an RMS voltage, denoted U_{rms}. In the case of a balanced three-phase system,

the relationship between the RMS line-to-neutral and line-to-line voltage is:

$$U_{\text{rms}} = \sqrt{3} V_{\text{rms}} \qquad \text{[A1.61]}$$

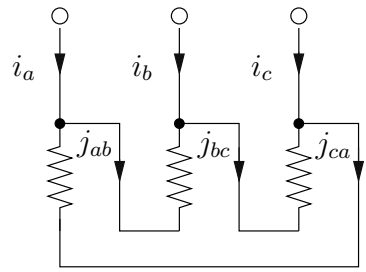


Figure A1.1. *Line and branch currents for a triangular connection*

A second point, which may lead to a different formulation of expression [A1.58], is concerned with currents. Generally speaking, we always have access to *line currents*, and thus to the RMS value I_{rms}. A second type of current can appear when using a load with a triangle connection (see Figure A1.1): this branch current presents an RMS value J_{rms} with the following expression as a function of I_{rms}:

$$J_{\text{rms}} = \frac{I_{\text{rms}}}{\sqrt{3}} \qquad \text{[A1.62]}$$

A1.4. Mathematics for electromagnetism

A1.4.1. *The Green–Ostrogradsky theorem*

The Green–Ostrogradsky theorem (also known as the flux–divergence theorem) establishes a connection between the integral of the divergence of a field with vector **E** in a

volume Ω and the integral of the flux of $\mathbf{E}$ on the closed surface $\partial\Omega$ delimiting the volume Ω:

$$\iiint_{\Omega} \mathrm{div}\mathbf{E}.d\omega = \oiint_{\partial\Omega} \mathbf{E} \cdot d\mathbf{s} \qquad [A1.63]$$

where $d\omega$ is a volume element, while $d\mathbf{s}$ is a normal vector[1] with a surface element (infinitesimal) ds of the complete surface $\partial\Omega$.

A1.4.2. *Stokes–Ampère theorem*

The Stokes–Ampère theorem establishes a connection between the the flux curl of the magnetic field $\mathbf{H}$ on a surface Σ and the integral of the circulation of $\mathbf{H}$ along the closed contour $\partial\Sigma$ delimiting surface Σ:

$$\iint_{\Sigma} \mathbf{curl}\,\mathbf{H} \cdot d\mathbf{s} = \oint_{\partial\Sigma} \mathbf{H} \cdot d\mathbf{l} \qquad [A1.64]$$

where $d\mathbf{s}$ is a normal vector[2] with a surface element (infinitesimal) ds of the complete surface Σ. Element $d\mathbf{l}$ is a vector (whose norm is dl) tangent to the closed contour $\partial\Sigma$.

A1.4.3. *Differential and referential operators*

The definition of the differential operators used in electromagnetism (primarily **grad**, div and **curl**) is dependent on the chosen frame of reference. Using the Cartesian

1 Oriented toward the outside of volume Ω.

2 Oriented in accordance with the right-hand rule as a function of the choice of orientation of contour $\partial\Sigma$.

coordinate system, the nabla operator (vector), ∇, allows us to easily write these operators as:

$$\nabla = \begin{pmatrix} \frac{\partial}{\partial x} \\ \frac{\partial}{\partial y} \\ \frac{\partial}{\partial z} \end{pmatrix} \qquad \text{[A1.65]}$$

and we know that:

$$\begin{cases} \mathbf{grad}\, V = \nabla V \\ \operatorname{div} \mathbf{E} = \nabla \cdot \mathbf{E} \\ \mathbf{curl}\, \mathbf{H} = \nabla \times \mathbf{H} \end{cases} \qquad \text{[A1.66]}$$

where the symbol "$\cdot$" is the scalar product and "$\times$" is the vector product.

If we want to write these operators using spherical or cylindrical coordinates, the ∇ operator is no longer suitable; in these cases, it is better to use intrinsic definitions (which are independent of the chosen frame of reference). For the gradient, we have:

$$dV = (\mathbf{grad}\, V) \cdot d\mathbf{r} \qquad \text{[A1.67]}$$

where dV is the exact total differential of V and dr is an infinitesimal shift (vector) away from the considered point in the space (defined by vector r from the origin of the reference frame).

For the "divergence" and "curl" operators, we simply use the two theorems presented in sections A1.4.1 and A1.4.2. First, we obtain:

$$d\phi = \operatorname{div} \mathbf{E}.d\omega \qquad \text{[A1.68]}$$

where $d\phi$ is the flux of $\mathbf{E}$ across the surface of the volume $d\omega$ under consideration.

We can then write:

$$d\mathcal{C} = \mathbf{curl}\,\mathbf{H} \cdot \mathbf{n}.d\mathcal{S} \qquad \text{[A1.69]}$$

where $d\mathcal{C}$ is the circulation of field H along a closed contour enclosing a surface $d\mathcal{S}$, and with an orientation allowing us to define a normal (unitary) vector $\mathbf{n}$ (in accordance with the right-hand rule).

Appendix 2

Elements of Spectral Analysis

A2.1. Periodic signals

A2.1.1. *Fourier series decomposition*

A Fourier series decomposition consists of writing a T-periodic signal $x(t)$ (i.e. with a frequency $F = 1/T$) as an infinite (discrete) sum of sinusoids with frequency $k.F$ (where $k \in \mathbb{N}$). This Fourier series decomposition is convergent at all points, on the condition that certain mathematical conditions are met; in this context, we will consider these conditions to be met by ensuring the continuity of signal $x(t)$. Mathematically speaking, in the opposite case, convergence is not guaranteed but is still "almost always" obtained[1]. Thus, we may use the following equation:

$$x\left(t\right) = a_0 + \sum_{k=1}^{+\infty} a_k.\cos\left(2\pi kF.t\right) + b_k.\sin\left(2\pi kF.t\right) \qquad \text{[A2.1]}$$

1 While this definition is simplistic from a mathematical perspective, it is largely sufficient when studying power electronics, and may be used more widely in electrical engineering.

where (taking $k > 1$):

$$a_0 = \frac{1}{T}\int_0^T x\left(t\right).dt \qquad \text{[A2.2]}$$

$$a_k = \frac{2}{T}\int_0^T x\left(t\right).\cos\left(2\pi kFt\right).dt \qquad \text{[A2.3]}$$

$$b_k = \frac{2}{T}\int_0^T x\left(t\right).\sin\left(2\pi kFt\right).dt \qquad \text{[A2.4]}$$

Note that the amplitude A_k of the sinusoid of frequency $k.F$ is obtained by combining the "cos" and "sin" terms, i.e.:

$$A_k = \sqrt{a_k^2 + b_k^2} \qquad \text{[A2.5]}$$

Another Fourier series formulation is possible, using the complex exponential $\mathrm{e}^{j2k\pi Ft}$, where $k \in \mathbb{Z}$, in the place of the "cos" and "sin" functions:

$$x(t) = \sum_{k=-\infty}^{+\infty} c_k.\mathrm{e}^{j2k\pi Ft} \qquad \text{[A2.6]}$$

with:

$$c_k = \frac{1}{T}\int_0^T x\left(t\right).\mathrm{e}^{j2k\pi Ft}.dt \qquad \text{[A2.7]}$$

Note that in this case the c_k coefficients of the Fourier series are complex numbers.

A2.1.2. *Properties*

A2.1.2.1. *Symmetries*

In the case of an even $x(t)$ signal, i.e. such that $x(-t) = x(t)$, it is easy to verify that:

$$\forall k \in \mathbb{N},\ b_k = 0 \qquad \text{[A2.8]}$$

For an odd $x(t)$ signal, such that $x(-t) = -x(t)$, it is easy to verify that:

$$\forall k \in \mathbb{N},\ a_k = 0 \qquad \text{[A2.9]}$$

More specifically, if we have symmetry "in $T/2$ and $T/4$", the Fourier series decomposition is simplified, with a reduction in the number of coefficients to calculate.

If (axial) symmetry exists in $T/2$, then the decomposition only includes non-null odd coefficients ($a_{2p} = b_{2p} = 0$).

In the same way, if (central) symmetry exists in $T/4$, then the odd coefficients which are multiples of 3 will be null (coefficients 3, 9, 15, etc.).

For example, consider the case of the waveform of the line-to-line voltage output of a three-phase inverter under "full wave" command (see Chapter 2, Figure 2.13, of this volume). In this case, both types of symmetry are present, and only the odd components which are not multiples of 3 will have non-null amplitudes. This is easy to verify for learning purposes.

More generally, we may wish to consider the properties of the complex Fourier series decomposition. In this case, we note that the ranks are relative integers (positive, negative or null), whereas in the case of a "cos/sin" breakdown, the ranks are always natural integers (positive or null). If the signal $x(t)$ is real (i.e. a function of $\mathbb{R}$ in $\mathbb{R}$)[2], the Fourier decomposition presents a property known as Hermitian symmetry, which consists of noting that:

$$\forall k \in \mathbb{Z},\ c_{-k} = c_k^* \qquad \text{[A2.10]}$$

2 This is the most common situation encountered in power electronics.

A2.1.2.2. *Integration / derivation*

The integration $\int x(t).dt$ and the derivation $\dot{x}(t)$ of a signal $x(t)$ with a known Fourier series decomposition allow immediate calculation of the Fourier series of $\int x(t).dt$ and $\dot{x}(t)$. If we consider the following complex decomposition of $x(t)$:

$$x(t) = \sum_{k=-\infty}^{+\infty} c_k.\mathrm{e}^{j2k\pi Ft} \qquad \text{[A2.11]}$$

we deduce:

$$\int x(t).dt = \sum_{k=-\infty}^{+\infty} \underbrace{\frac{c_k}{j2k\pi F}}_{\gamma_k} \cdot \mathrm{e}^{j2k\pi Ft} \qquad \text{[A2.12]}$$

and:

$$\dot{x}(t) = \sum_{k=-\infty}^{+\infty} \underbrace{j2k\pi F.c_k}_{\delta_k} \cdot \mathrm{e}^{j2k\pi Ft} \qquad \text{[A2.13]}$$

A2.1.2.3. *Temporal dilation / contraction*

Temporal dilation or contraction consists of transforming an initial signal $x(t)$ into a signal $x(a.t)$ where $a \in \mathbb{R}^{+*}$. This type of transformation has no effect on the Fourier series decomposition or the way in which it is calculated. We must simply remember that the fundamental frequency $F = 1/T$ has been modified (along with the harmonics $k.F$), becoming $a.F$ (respectively, $a.k.F$).

A2.1.3. *Parseval's theorem*

The RMS value X_{rms} of a signal $x(t)$ may be obtained by direct integration, applying the following definition:

$$X_{\mathrm{rms}}^2 = \frac{1}{T}\int_0^T x^2\,(t)\,.dt \qquad \text{[A2.14]}$$

This is also possible using a link to coefficients a_0 and c_k of the Fourier series:

$$X_{\text{rms}}^2 = a_0^2 + \sum_{k=1}^{+\infty} \left(a_k^2 + b_k^2\right) = \sum_{k=-\infty}^{+\infty} c_k.c_k^* \qquad \text{[A2.15]}$$

This formula is known as Parseval's theorem.

A2.1.4. *Total harmonic distortion*

Parseval's theorem is extremely useful for calculating the total harmonic distortion (THD) of a non-sinusoidal value which we wish to compare to a pure sinusoid.

Two definitions of THD are used in two different standards:

– $\text{THD} - \text{F}$ (IEEE or DIN standards) related to the fundamental of the value (which may be greater than 1):

$$\text{THD} - \text{F} = \frac{\sqrt{\sum_{k=2}^{+\infty} \left(a_k^2 + b_k^2\right)}}{\sqrt{a_1^2 + b_1^2}}; \qquad \text{[A2.16]}$$

– the $\text{TDH} - \text{F}$ (IEC standard) related to the overall RMS value (always less than or equal to 1):

$$\text{THD} - \text{F} = \frac{\sqrt{\sum_{k=2}^{+\infty} \left(a_k^2 + b_k^2\right)}}{\sqrt{\sum_{k=1}^{+\infty} \left(a_k^2 + b_k^2\right)}}. \qquad \text{[A2.17]}$$

REMARK A2.1.– Note that, as a general rule, $\text{TDH} - \text{F}$ ($\text{X} = \text{F}$ or G) is calculated using quantities with a null continuous component (i.e. for $a_0 = 0$) or at least that the continuous component is not taken into account in calculating the THD.

A2.2. Double Fourier series and PWM

A2.2.1. *Context of study*

Before considering the spectral analysis of non-periodic signals, which will be covered in section A2.3, we will focus on one particularly important class of periodic signals encountered in power electronics: MLI signals, obtained by the modulation of a triangular (or sawtooth) carrier of frequency F_d using a periodic modulation sequence (not necessarily sinusoidal) of frequency F_m. The effective determination of a Fourier series in this case is subject to significant calculation problems. The desired result may be obtained using a method based on a double Fourier series, proposed in [BEN 33] in 1933 and in [BLA 53] in 1953.

A2.2.2. *Double Fourier series*

The double Fourier series is a generalization of the Fourier series to periodic functions of two variables of the type $f(x,y)$, with a period of 2π along the two axes[3]. As in the case of [A2.1], it is possible to write:

$$\begin{aligned} f(x,y) = A_{00} &+ \sum_{n=1}^{\infty} \left(A_{0n}.\cos(ny) + B_{0n}.\sin(ny)\right) \\ &+ \sum_{m=1}^{\infty} \left(A_{m0}.\cos(mx) + B_{m0}.\sin(mx)\right) \\ &+ \sum_{n=1}^{\infty} \sum_{m=\pm 1}^{\pm\infty} \left(A_{mn}.\cos(mx+ny)\right. \\ &\left. + B_{mn}.\sin(mx+ny)\right) \end{aligned} \qquad \text{[A2.18]}$$

where $\forall m \in \mathbb{N}, n \in \mathbb{Z}$:

$$A_{mn} = \frac{1}{2\pi^2} \int_0^{2\pi} \int_0^{2\pi} f(x,y).\cos(mx+ny).dx.dy \qquad \text{[A2.19]}$$

3 This does not limit the generality of the method, as this specific case can always be attained by changing a variable.

and:

$$B_{mn} = \frac{1}{2\pi^2} \int_0^{2\pi} \int_0^{2\pi} f(x,y) \,.\, \sin(mx + ny) \,.dx.dy \quad \text{[A2.20]}$$

A2.2.3. *PWM and the "wall model"*

The "wall model" is based on the duplication of a time motif in the modulator across a series of vertical bands, with a width equal to the amplitude of the carrier, as shown in Figure A2.1. In this case, we will consider the simplest possibility using a sawtooth carrier: this type of carrier corresponds to an oblique line (AB) cutting across the copies, with regular modulator steps, for each switching instant of the PWM signal $c_{pwm}(t)$ for which we wish to calculate the spectrum. We must simply note that, when this line "travels through" the hatched zones, $c_{pwm} = 1$; in the white zones, $c_{pwm} = 0$.

Based on this representation, it is evidently possible to define a function $f(x,y)$ such that:

$$f(x,y) = \begin{cases} 1 \text{ in the hatched zone} \\ 0 \text{ otherwise} \end{cases} \quad \text{[A2.21]}$$

This function is periodic along both axes by construction: it can, therefore, be decomposed to produce a double Fourier series, as described in section A2.2.2. Finally, we must simply analyze the spectrum obtained along the line (AB) to obtain the RMS spectrum of the PWM signal. To do this, we note the relationship between variable $x = \omega_m t$ and $y = \omega_d t$[4] to obtain the desired result.

4 With these two variables x and y, function $f(x,y)$ is 2π-periodic along both axes.

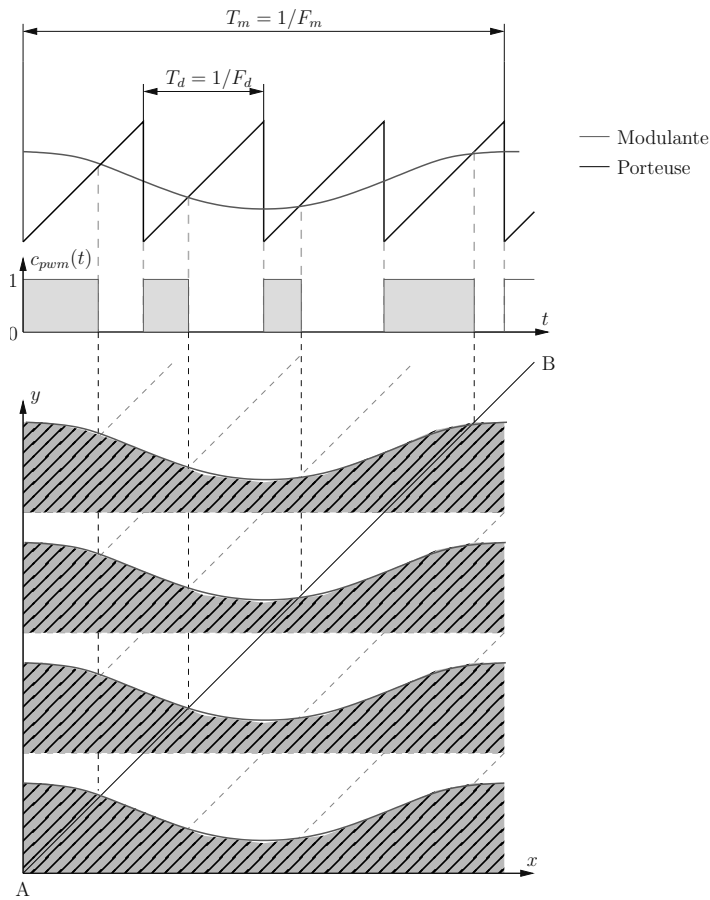


Figure A2.1. *Creation of a two-dimensional function for Fourier series decomposition. For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

REMARK A2.2.– This particularly elegant method avoids the (major) difficulty of direct calculation of a PWM spectrum. However, the calculation is still relatively cumbersome, and involves Bessel functions of the first time, which can only be calculated approximately. We then simply read the curves produced by this family of functions to obtain an exact spectral representation of a given PWM signal.

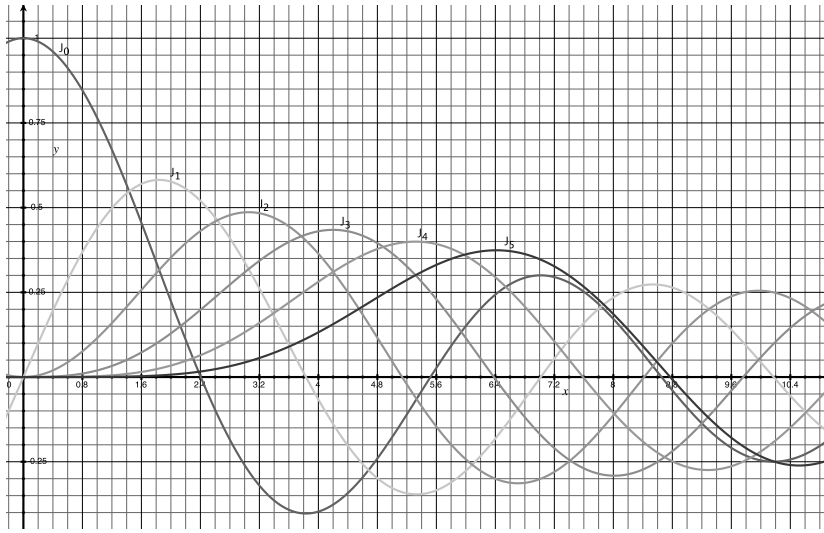


Figure A2.2. *Bessel functions of the first kind of order 0–5. For a color version of the figure, see www.iste.co.uk/patin/power2.zip*

A2.2.4. *Bessel functions*

The Bessel function of the first kind of order n is defined by the general formula:

$$J_n(x) = \frac{j^{-n}}{2\pi} \int_0^{2\pi} e^{jx\cos(\alpha)} e^{jn\cdot\alpha} d\alpha \qquad \text{[A2.22]}$$

The effective determination of the value of a Bessel function for any given argument is generally based on numerical calculations, or by reading the curves presented in Figure A2.2.

A2.2.5. *Analytical spectra for different PWMs*

In this section, we will consider the Fourier series decompositions of a number of widespread PWM signal types:

– PWM with unipolar sawtooth (increasing) carrier;

– PWM with bipolar sawtooth (increasing) carrier;

– PWM with unipolar triangular (symmetrical) carrier;

– PWM with bipolar triangular carrier.

When noting PWM parameters, we will consider that the modulator (presumed, in this case, to be sinusoidal) takes the following form:

$$m(t) = M_0 + M_{\max}.\cos(\omega_m t + \phi_{m0}) \qquad \text{[A2.23]}$$

The carrier has a peak-to-peak amplitude $P_{\max}$ and may be unipolar (varying between 0 and $P_{\max}$) or bipolar (varying between $-P_{\max}$ and $P_{\max}$), of frequency F_d. Note that a distinction is commonly made between the definitions of the PWM signal c_{pwm} in these two cases:

– for unipolar PWM, $c_{pwm} \in \{0, 1\}$;

– for bipolar PWM, $c_{pwm} \in \{-1/2, 1/2\}$ (but this may also be $\{-1, 1\}$).

Using these bases, we can define an average PWM signal $c_0 = \frac{M_0}{P_{\max}}$, whatever the strategy (unipolar or bipolar) and the depth of modulation $m = \frac{2M_{\max}}{P_{\max}}$ (once again, this is independent of the modulation type).

REMARK A2.3.– Using PWM signals with a unitary peak-to-peak amplitude for unipolar and bipolar PWM strategies makes it easier to carry out comparisons.

Furthermore, the instantaneous phase of the carrier is denoted as $\phi_p(t) = \omega_p t + \phi_{p0}$ where $\omega_p = 2\pi F_p$.

More information on PWM spectra may be found in [BLA 53], which also covers the case of decreasing sawtooth carriers.

A2.2.5.1. *PWM with a unipolar sawtooth carrier*

In this case, the signal c_{pwm} is decomposed as follows:

$$\begin{aligned} c_{pwm}(t) = c_0 &+ \frac{m}{2}\cos(\omega_m t + \phi_{m0}) \\ &+ \sum_{k=1}^{\infty} \frac{1}{k\pi} \left[\sin(k(\omega_p t + \phi_{p0})) \right. \\ &\left. - J_0(km\pi).\sin(k(\omega_p t + \phi_{p0}) - 2kc_0\pi)\right] \\ &+ \sum_{k=1}^{\infty} \sum_{l=\pm 1}^{\pm\infty} \frac{J_l(km\pi)}{k\pi} \sin\left(\frac{l\pi}{2} - k(\omega_p t + \phi_{p0})\right. \\ &\left. - l(\omega_m t + \phi_{m0}) + 2kc_0\pi\right) \end{aligned} \qquad \text{[A2.24]}$$

where we usually have $c_0 = 1/2$.

A2.2.5.2. *PWM with a bipolar sawtooth carrier*

In this case, we have (for $c_0 = 0$):

$$\begin{aligned} c_{pwm}(t) = &\frac{m}{2}\cos(\omega_m t + \phi_{m0}) \\ &+ \sum_{k=1}^{\infty} \frac{1}{k\pi} \left[\cos(k\pi) - J_0(km\pi).\sin(k(\omega_p t + \phi_{p0}))\right] \\ &+ \sum_{k=1}^{\infty} \sum_{l=\pm 1}^{\pm\infty} \frac{J_l(km\pi)}{k\pi} \sin\left(\frac{l\pi}{2} - k(\omega_p t + \phi_{p0})\right. \\ &\left. - l(\omega_m t + \phi_{m0})\right) \end{aligned} \qquad \text{[A2.25]}$$

A2.2.5.3. *PWM with a unipolar triangular carrier*

Using this new carrier, we obtain:

$$\begin{aligned} c_{pwm}(t) = c_0 &+ \frac{m}{2}\cos(\omega_m t + \phi_{m0}) \\ &+ \sum_{k=1}^{\infty} \frac{2}{k\pi} \cdot J_0\left(\frac{km\pi}{2}\right) \cdot \sin(k\pi c_0)\cos(k(\omega_p t + \phi_{p0})) \end{aligned}$$

$$+\sum_{k=1}^{\infty}\sum_{l=\pm 1}^{\pm\infty}\frac{2}{k\pi}\cdot J_l\left(\frac{km\pi}{2}\right)$$
$$\cdot\sin\left(\frac{(2kc_0+l)\,\pi}{2}\right)\cos\left(k\left(\omega_p t+\phi_{p0}\right)+l\left(\omega_m t+\phi_{m0}\right)\right) \quad \text{[A2.26]}$$

As in the case of PWM with a unipolar sawtooth carrier, we generally take $c_0 = 1/2$.

A2.2.5.4. *PWM with a bipolar triangular carrier*

In this final case, we obtain (for $c_0 = 0$):

$$\begin{aligned} c_{pwm}(t) = {} & \frac{m}{2}\cos\left(\omega_m t+\phi_{m0}\right) \\ & +\sum_{k=1}^{\infty}\frac{2}{k\pi}\cdot J_0\left(\frac{km\pi}{2}\right)\cdot\sin\left(\frac{k\pi}{2}\right)\cos\left(k\left(\omega_p t+\phi_{p0}\right)\right) \\ & +\sum_{k=1}^{\infty}\sum_{l=\pm 1}^{\pm\infty}\frac{2}{k\pi}\cdot J_l\left(\frac{km\pi}{2}\right) \\ & \cdot\sin\left(\frac{(k+l)\,\pi}{2}\right)\cos\left(k\left(\omega_p t+\phi_{p0}\right)+l\left(\omega_m t+\phi_{m0}\right)\right) \end{aligned}$$

[A2.27]

A2.2.5.5. *Qualitative summary*

In practice, triangular carrier PWMs are less rich in harmonic components (at least around frequency F_d) than those using a sawtooth carrier. Furthermore, unipolar PWM, for which we use voltage levels of 0 and U_0 during the positive alternations of the modulator and 0 and $-U_0$ for negative alternations, produces spectral content which is less rich than that produced by bipolar PWM (with the use of $\pm U_0$ over a switching period): this point is clearly illustrated in Chapter 2 of this volume.

A2.3. Non-periodic signals

A2.3.1. *Fourier transformation*

Fourier series can be extended to non-periodic signals using the notion of Fourier transformation. Any given signal $x(t)$ is associated with a Fourier transform $\mathcal{X}(f)$ defined as follows:

$$\mathcal{X}(f) = \mathcal{F}[x(t)] = \int_{\mathbb{R}} x(t).\mathrm{e}^{-j2\pi ft}.dt \qquad \text{[A2.28]}$$

A2.3.2. *The Dirac impulse*

The unitary element of the Fourier transformation is a Dirac impulse $\delta(t)$. This is a distribution (generalization of mathematical functions) which can be assimilated, from a physical perspective, to a passage at the limit of a "gateway" function $\pi_T(t)$, defined as follows:

$$\pi_T(t) = \begin{cases} \frac{1}{T} \text{ pour } |t| \leq T/2 \\ 0 \text{ for } |t| > T/2 \end{cases} \qquad \text{[A2.29]}$$

Note, based on this definition, that:

$$\forall T \in \mathbb{R}^{+*}, \int_{\mathbb{R}} \pi_T(t).dt = 1 \qquad \text{[A2.30]}$$

The passage at the limit value leading to the Dirac impulse is thus:

$$\delta(t) = \lim_{T \to 0} \pi_T(t) \qquad \text{[A2.31]}$$

One important property of the Dirac impulse in the case of a function f(t) which is continuous in 0 is that:

$$\int_{\mathbb{R}} \delta(t).f(t).dt = f(0) \qquad \text{[A2.32]}$$

This enables us to establish the Fourier transform of the Dirac impulse $\Delta(f) = \mathcal{F}[\delta(t)]$:

$$\Delta(f) = 1 \qquad \text{[A2.33]}$$

Thus, we see that the spectral content of this impulse is uniform, and the spectral range is infinite. This is simply a mathematical tool, which has no physical reality in absolute terms: a Dirac impulse is impossible to obtain in practice, but remains useful for simplified modeling of brief events (which may be considered to be instantaneous[5] for the purposes of initial analysis).

A2.3.3. *Properties*

A2.3.3.1. *Linearity*

As the Fourier transformation is an integral, its linearity is easy to verify:

$$\forall(\lambda,\mu)\in\mathbb{R}^2, \mathcal{F}[\lambda.p(t)+\mu.q(t)] = \lambda.\mathcal{F}[p(t)]+\mu.\mathcal{F}[q(t)] \qquad \text{[A2.34]}$$

A2.3.3.2. *Integration / derivation*

Let us consider a signal $x(t)$, with a known Fourier transform denoted as $\mathcal{X}(f) = \mathcal{F}[x(t)]$. We will begin by establishing the expression of the Fourier transform of $\int_{-\infty}^{t} x(\tau).d\tau$:

$$\mathcal{F}\left[\int_{-\infty}^{t} x(\tau).d\tau\right] = \int_{\mathbb{R}}\int_{-\infty}^{t} x(\tau).d\tau.\mathrm{e}^{-j2\pi ft}.dt \qquad \text{[A2.35]}$$

REMARK A2.4.– The formula for integration by parts can be deduced from the product derivation formula:

$$(uv)' = u'v + uv' \qquad \text{[A2.36]}$$

5 Switching, for example, in the context of power electronics.

This gives us the following result:

$$\int uv' = [uv] - \int u'v \qquad \text{[A2.37]}$$

Using [A2.37], based on [A2.35], we obtain the following result:

$$\mathcal{F}\left[\int_{-\infty}^{t} x(\tau).d\tau\right] = \left[\int_{-\infty}^{t} x(\tau).d\tau \cdot \frac{\mathrm{e}^{-j2\pi ft}}{-j2\pi f}\right]_{-\infty}^{+\infty} + \frac{1}{j2\pi f} \cdot \int_{\mathbb{R}} x(t).\mathrm{e}^{-j2\pi ft}.dt \qquad \text{[A2.38]}$$

Supposing that the integrated function tends toward zero toward infinity (i.e. in $\pm\infty$), the first term disappears. Hence:

$$\mathcal{F}\left[\int_{-\infty}^{t} x(\tau).d\tau\right] = \frac{1}{j2\pi f} \cdot \int_{\mathbb{R}} x(t).\mathrm{e}^{-j2\pi ft}.dt = \frac{\mathcal{X}(f)}{j2\pi f} \qquad \text{[A2.39]}$$

For derivation, we wish to calculate the Fourier transform of $\dot{x}(t) = \frac{dx}{dt}$:

$$\mathcal{F}[\dot{x}(t)] = \int_{\mathbb{R}} \dot{x}(t).\mathrm{e}^{-j2\pi ft}.dt \qquad \text{[A2.40]}$$

Similarly to the case of integration, we can establish the following relationship (using integration by parts):

$$\mathcal{F}[\dot{x}(t)] = j2\pi f.\mathcal{X}(f) \qquad \text{[A2.41]}$$

A2.3.3.3. *Temporal dilatation / contraction*

The problem of temporal dilation and contraction for the Fourier transform is different from that encountered using Fourier series for periodic signals. However, the starting point for study still consists of replacing a signal $x(t)$ with a known Fourier transform $\mathcal{X}(f)$ by a signal $x(a.t)$ with a

strictly positive real coefficient a (i.e. $a \in \mathbb{R}^{+*}$). We may begin by defining the Fourier transform of the new signal:

$$\mathcal{F}\left[x\left(a.t\right)\right] = \int_{\mathbb{R}} x\left(a.t\right).\mathrm{e}^{-j2\pi ft}.dt \qquad \text{[A2.42]}$$

We then simply change a variable ($\tau = a.t$ and thus $t = \frac{\tau}{a}$) to obtain a result. First, note that $dt = \frac{d\tau}{a}$; as $a > 0$, integration is always carried out from $-\infty$ to $+\infty$ (and not in the opposite direction). Hence:

$$\mathcal{F}\left[x\left(a.t\right)\right] = \frac{1}{a}\mathcal{X}\left(\frac{f}{a}\right) \qquad \text{[A2.43]}$$

A2.3.3.4. *Hermitian symmetry*

Hermitian symmetry, as seen in the context of complex Fourier series, also occurs in the case of the Fourier transform. When the signal $x(t)$ under study is real, symmetry will be present between the value of the Fourier transform $\mathcal{X}\left(f\right)$ in f and in $-f$. This is why the representation of a signal spectrum is generally limited to a unilateral representation for $f \geq 0$, and not to the bilateral form, which provides no additional information. To demonstrate this symmetry, note the expression of the Fourier transform of $x(t)$:

$$\mathcal{X}(f) = \int_{\mathbb{R}} x(t).\mathrm{e}^{-j2\pi ft}.dt \qquad \text{[A2.44]}$$

The conjugation operation (denoted as$\mathrm{conj}(z) = z^*$) is linear and can consequently be placed inside or outside of the $\int$ sign. Thus:

$$\mathcal{X}(f)^* = \left(\int_{\mathbb{R}} x(t).\mathrm{e}^{-j2\pi ft}.dt\right)^* = \int_{\mathbb{R}} \left(x(t).\mathrm{e}^{-j2\pi ft}\right)^*.dt \qquad \text{[A2.45]}$$

The conjugation of a product is equal to the product of the conjugations:

$$\mathcal{X}(f)^* = \int_{\mathbb{R}} x(t)^*.\mathrm{e}^{j2\pi ft}.dt \qquad \text{[A2.46]}$$

If $x(t)$ is real, we have $x(t) = x(t)^*$ and thus:

$$\mathcal{X}(f)^* = \int_{\mathbb{R}} x(t).\mathrm{e}^{j2\pi ft}.dt = \mathcal{X}(-f) \qquad \text{[A2.47]}$$

This result is known as the Hermitian symmetry of a Fourier transform (of a real signal), and corresponds to the continuous form of result [A2.10], obtained for complex Fourier series.

A2.3.3.5. *Time reversal*

We have already considered the impact of temporal dilation/contraction on the Fourier transform of a signal, using a strictly positive temporal modification coefficient ($a > 0$). We may also wish to consider the case where a is negative (non-null), or the specific case where signal $x(t)$ is replaced by an opposite signal in relation to the time axis $x(-t)$. Note that the composition of the two effects produces a general case, corresponding to $a \in \mathbb{R}^*$:

$$\mathcal{F}[x(-t)] = \int_{\mathbb{R}} x(-t).\mathrm{e}^{-j2\pi ft}.dt \qquad \text{[A2.48]}$$

Once again, we must change a variable ($\tau = -t$, and thus $dt = -d\tau$). Note that, in this case, the direction of integration is also reversed:

$$\begin{aligned}\mathcal{F}[x(-t)] &= -\int_{+\infty}^{-\infty} x(\tau).\mathrm{e}^{j2\pi f\tau}.d\tau = \int_{-\infty}^{+\infty} x(\tau).\mathrm{e}^{j2\pi f\tau}.d\tau \\ &= \mathcal{X}(-f) \qquad \text{[A2.49]}\end{aligned}$$

Based on the Hermitian symmetry result established in the previous section, we obtain:

$$\mathcal{F}\left[x\left(-t\right)\right] = \mathcal{X}\left(f\right)^{*} \qquad \text{[A2.50]}$$

A2.3.3.6. *Lag*

When a signal $x(t)$ with a known Fourier transform $\mathcal{X}(f)$ is delayed for a duration t_0, we can easily verify, by changing a variable, that:

$$\mathcal{F}\left[x\left(t-t_0\right)\right] = \mathcal{X}\left(f\right).\mathrm{e}^{-j2\pi f t_0} \qquad \text{[A2.51]}$$

A2.3.3.7. *Frequency translation*

When we multiply a signal $x(t)$ with a known Fourier transform $\mathcal{X}(f)$ by a complex exponential $\mathrm{e}^{j2\pi f_0 t}$, it is possible to show that the convolution in terms of frequency leads to a frequency translation:

$$\mathcal{F}\left[x\left(t\right).\mathrm{e}^{j2\pi f_0 t}\right] = \mathcal{X}\left(f-f_0\right) \qquad \text{[A2.52]}$$

A2.3.3.8. *Convolution*

The convolution product $\star$ is a mathematical operation which is widely used in physics in relation to the solution of ordinary differential equations (the tool may also be generalized for the solution of partially derived equations, with the addition of a Green node). Unfortunately, this operation is hard to process directly in practice, as it concerns the "sliding" integral of the product of two functions between $-\infty$ and $+\infty$, as demonstrated by the following definition:

$$r(t) = \left(p \star q\right)\left(t\right) = \int_{\mathbb{R}} p\left(\tau\right).q\left(t-\tau\right).d\tau \qquad \text{[A2.53]}$$

However, this operation may be carried out in a simplified manner in an image domain: the Fourier (frequency) domain, and more generally the Laplace domain (used in automatics,

and discussed in Volume 3 [PAT 15b], Chapter 4, in the context of switch-mode power supply transfer), may be treated by introducing the Laplace variable p. The simplification operation consists of noting that the convolution product becomes a simple product (i.e. an arithmetic multiplication) in this image domain.

Let us consider two signals $p(t)$ and $q(t)$, with Fourier transforms denoted as $\mathcal{P}(f)$ and $\mathcal{Q}(f)$, respectively. The product of convolution $r(t)$ between $p(t)$ and $q(t)$, defined in accordance with equation [A2.53], presents a Fourier transform $\mathcal{R}(f)$ which may be expressed using the following formula:

$$\mathcal{R}(f) = \mathcal{P}(f).\mathcal{Q}(f) \qquad \text{[A2.54]}$$

Note that, while this result appears to be simple, a (potentially considerable) difficulty remains concerning the return to the temporal domain. To do this, we need to use an inverse Fourier transformation formula, and we must be able to apply this formula to the result obtained in [A2.54].

In the case where one of the two functions is replaced by the Dirac impulse, which is the neutral element of the convolution product (here, using any given function $f(t)$), calculation is simple:

$$(f \star \delta)(t) = (\delta \star f)(t) = f(t) \qquad \text{[A2.55]}$$

This is also valid in the frequency domain, as the Fourier transform $\Delta(f)$ of the Dirac impulse has a value of 1, as demonstrated in [A2.33].

REMARK A2.5.– The Fourier transform allows us to replace the convolution product by a simple product, as shown above, but the reverse is also true. A simple product may be replaced by a convolution product using a Fourier transformation.

A2.3.3.9. *Inverse transformation*

The inverse Fourier transformation will be defined below. In this case, consider a Fourier transform $\mathcal{X}(f)$ from which we wish to obtain the temporal original $x(t)$:

$$x(t) = \int_{\mathbb{R}} \mathcal{X}(f) . \mathrm{e}^{j2\pi ft} . df \qquad [A2.56]$$

REMARK A2.6.– The inverse Fourier transformation formula is very similar to the direct transformation formula, and its properties are similar, notably in relation to the convolution product.

A2.3.3.10. *Sinusoids*

The Fourier transform of $\cos(2\pi f_0 t)$ can be obtained using Euler's formula:

$$\cos(2\pi f_0 t) = \frac{\mathrm{e}^{j2\pi f_0 t} + \mathrm{e}^{-j2\pi f_0 t}}{2} \qquad [A2.57]$$

Consequently, the Fourier transformation gives us the following result:

$$\mathcal{F}[\cos(2\pi f_0 t)] = \frac{1}{2} \int_{\mathbb{R}} \left(\mathrm{e}^{-j2\pi(f-f_0)t} + \mathrm{e}^{-j2\pi(f+f_0)t} \right) . dt \qquad [A2.58]$$

A useful result consists of noting, based on [A2.33] and [A2.56], that:

$$\int_{\mathbb{R}} \mathrm{e}^{j2\pi ft} . df = \delta(t) \qquad [A2.59]$$

In the same way, as $\delta(t)$ is even, we may also write:

$$\int_{\mathbb{R}} \mathrm{e}^{-j2\pi ft} . df = \delta(t) \qquad [A2.60]$$

Note also that the roles of t and f are completely interchangeable in these results.

Consequently, after changing the variable, we obtain:

$$\mathcal{F}\left[\cos\left(2\pi f_0 t\right)\right] = \frac{1}{2}\left(\delta\left(f - f_0\right) + \delta\left(f + f_0\right)\right) \qquad \text{[A2.61]}$$

In the case of the signal $\sin\left(2\pi f_0 t\right)$, we begin by noting:

$$\sin\left(2\pi f_0 t\right) = \frac{\mathrm{e}^{j2\pi f_0 t} - \mathrm{e}^{-j2\pi f_0 t}}{2j} \qquad \text{[A2.62]}$$

We then deduce the spectrum, as in the case of [A2.61]:

$$\mathcal{F}\left[\cos\left(2\pi f_0 t\right)\right] = \frac{1}{2j}\left(\delta\left(f - f_0\right) - \delta\left(f + f_0\right)\right) \qquad \text{[A2.63]}$$

REMARK A2.7.– We see that Hermitian symmetry, as described in [A2.47], is respected for the two results [A2.61] and [A2.63].

A2.3.4. *Fourier transform of periodic signals*

Using the Fourier transform of any periodic signal, we may expect to obtain a discrete spectrum (non-null only at multiples of the fundamental frequency), corresponding to the complex Fourier series decomposition.

Let us consider a signal $m_T(t)$ with a finite temporal support T (i.e. non-null for an interval of width T alone). It is interesting to note that the convolution of this signal by a delayed Dirac impulse $\delta_{t_0}\left(t\right) = \delta\left(t - t_0\right)$ gives us a delayed version of the signal:

$$\left(m_T \star \delta_{t_0}\right)\left(t\right) = m_T\left(t - t_0\right) \qquad \text{[A2.64]}$$

Based on this result, a T-periodic signal $m(t)$ may be formed using the motif $m_T(t)$ using convolution between this initial signal and a Dirac comb (sampling function) of period T:

$$\perp_T\left(t\right) = \sum_{k\in\mathbb{Z}} \delta\left(t - kT\right) \qquad \text{[A2.65]}$$

Hence:

$$m(t) = (m_T \star \perp_T (t)) \qquad \text{[A2.66]}$$

Next, if we wish to calculate the Fourier transform $\mathcal{M}(f)$ of the obtained signal, we have:

$$\mathcal{M}(f) = \mathcal{M}_T(f) .\mathcal{F}\left[\sum_{k\in\mathbb{Z}} \delta(t - kT)\right] \qquad \text{[A2.67]}$$

As the Fourier transformation is a linear operation, it may be applied to each element under the $\sum$ sign separately:

$$\mathcal{M}(f) = \mathcal{M}_T(f) . \sum_{k\in\mathbb{Z}} \mathcal{F}[\delta(t - kT)] \qquad \text{[A2.68]}$$

Using [A2.33] and [A2.51], we have:

$$\mathcal{F}[\delta(t - kT)] = \mathrm{e}^{-j2k\pi fT} \qquad \text{[A2.69]}$$

Hence:

$$\mathcal{M}(f) = \mathcal{M}_T(f) . \sum_{k\in\mathbb{Z}} \mathrm{e}^{-j2k\pi fT} \qquad \text{[A2.70]}$$

The (frequency) periodicity $1/T$ of $X(f) = \sum_{k\in\mathbb{Z}} \mathrm{e}^{-j2k\pi fT}$ is easy to demonstrate. This spectrum may then be decomposed to produce a Fourier series. Moreover, this expression corresponds precisely to a complex decomposition in which all of the coefficients c_k (for any relative integer k) have a value of 1. For a signal $x(t)$, coefficient c_k is expressed as:

$$c_k = \frac{1}{T}\int_0^T x(t) .\mathrm{e}^{j2k\pi Ft} .dt \qquad \text{[A2.71]}$$

In the case of our frequency (with period $1/T$), this corresponds to:

$$c_k = T.\int_0^{1/T} X\left(f\right).\mathrm{e}^{j2k\pi Tf}.df \qquad \text{[A2.72]}$$

The integration interval should be of width $1/T$, but the boundaries may be modified: for example, we may choose an interval centered on $f = 0$ (between $-\frac{1}{2T}$ and $\frac{1}{2T}$). In this case, we wish to find a function $X(f)$ such that:

$$\forall k \in \mathbb{Z},\ c_k = 1 \qquad \text{[A2.73]}$$

It is easy to verify that:

$$X\left(f\right) = \frac{1}{T} \cdot \delta\left(f\right) \qquad \text{[A2.74]}$$

is a solution in the interval $\left[-\frac{1}{2T}; \frac{1}{2T}\right]$. Its existence is, therefore, proved, and in this case, unique. Consequently, the global expression of $X(f)$ (i.e. $\forall f \in \mathbb{R}$) is:

$$X\left(f\right) = \frac{1}{T} \cdot \sum_{k\in\mathbb{Z}} \delta\left(f - \frac{k}{T}\right) \qquad \text{[A2.75]}$$

We see that the spectrum of a temporal Dirac comb is a Dirac frequency comb. Expression [A2.70] of the spectrum of a periodic signal becomes:

$$\mathcal{M}\left(f\right) = \frac{1}{T} \cdot \mathcal{M}_T\left(f\right) . \sum_{k\in\mathbb{Z}} \delta\left(f - \frac{k}{T}\right) \qquad \text{[A2.76]}$$

We see that the continuous spectrum of the elementary motif $m_T(t)$ (defined over a single period T) is sampled at all multiples of the fundamental frequency $1/T$. This result is perfectly coherent with the expected discrete spectrum, and conforms to the complex Fourier series decomposition defined in [A2.6]–[A2.7].

A2.3.5. *Fourier transform of sampled signals*

The result presented in the previous section has a counterpart associated with the Fourier transform of a sampled signal. It is possible to demonstrate that a sampled signal (with discrete temporal components) is associated with a periodic frequency spectrum.

To do this, we associate a signal $x(t)$ with its sampled version $x^*(t)$, obtained by multiplying $x(t)$ by a temporal Dirac comb of period T:

$$x^*(t) = x(t).\sum_{k\in\mathbb{Z}} \delta\left(t - kT\right) \qquad \text{[A2.77]}$$

The Fourier transform $X^*(f)$ of this signal is obtained by convolution of spectrum $X(f)$ of $x(t)$ by the spectrum of the temporal Dirac comb:

$$X^*\left(f\right) = X\left(f\right) \star \mathcal{F}\left[\sum_{k\in\mathbb{Z}} \delta\left(t - kT\right)\right] \qquad \text{[A2.78]}$$

As the Fourier transform is a linear operation, we have:

$$\mathcal{F}\left[\sum_{k\in\mathbb{Z}} \delta\left(t - kT\right)\right] = \sum_{k\in\mathbb{Z}} \mathcal{F}\left[\delta\left(t - kT\right)\right] = \sum_{k\in\mathbb{Z}} \mathrm{e}^{-j2k\pi fT} \qquad \text{[A2.79]}$$

Therefore, we can write:

$$X^*\left(f\right) = X\left(f\right) \star \sum_{k\in\mathbb{Z}} \mathrm{e}^{-j2k\pi fT} \qquad \text{[A2.80]}$$

Note that $\sum_{k\in\mathbb{Z}} \mathrm{e}^{-j2k\pi fT}$ also appeared in equation [A2.70], where it was identified as a Dirac frequency comb. In this

case, the spectrum is convolved with $X(f)$, giving the following result:

$$X^*(f) = \sum_{k\in\mathbb{Z}} X\left(f - \frac{k}{T}\right) \qquad \text{[A2.81]}$$

The spectrum of the sampled signal is thus a duplication of the spectrum of the initial signal $x(t)$ around each multiple of the sampling frequency $1/T$. Note that if the spectrum $X(f)$ is bounded by a maximum frequency denoted as $f_{\max}$, the inequality $2f_{\max} \leq 1/T$ must be respected to avoid overlap in the duplicated motifs of spectrum $X(f)$. This inequality is known as Shannon's theorem and the overlap phenomenon is known as aliasing. This result is important not only in digital signal processing but also in explaining certain phenomena encountered in PWM, particularly the appearance of subharmonics when the switching frequency is too low in relation to the modulation frequency.

A2.3.6. *Parseval's theorem*

As for Fourier series, Parseval's theorem is applicable to Fourier transformations. However, there is one important nuance in this case: in the case of periodic signals, the integration interval for the square of the signal is limited to the period, whereas in the context of the Fourier transformation, the integration interval covers the whole of the real axis. The treated function must, therefore, be of class $\mathcal{L}_2$ (i.e. a summable square function).

Let us take a signal of this type, $x(t)$ (presumed to be complex in this case to ensure generality). An identity exists between the temporal and frequency integrals:

$$\int_{\mathbb{R}} |x(t)|^2 .dt = \int_{\mathbb{R}} |\mathcal{X}(f)|^2 .df \qquad \text{[A2.82]}$$

A2.3.7. *The Heisenberg–Gabor spectrum inequality*

The result presented here provides an important basis not only for signal theory, but also for quantum mechanics, where it is known as the Heisenberg uncertainty principle (established in 1927); Heisenberg was awarded the Nobel prize in physics in 1933 for creating this new area of research.

In qualitative terms, the result may be summarized as follows: a short signal (in temporal terms) occupies a broad range of frequencies. However, a signal which is highly localized in terms of frequency is longer in terms of time.

This result is clearly shown in two of the examples seen above:

– The Dirac impulse is the shortest possible signal, and, as we have seen, its spectrum is uniform up to $f \to \infty$.

– The sinusoid (with frequency f_0) is a signal with a spectrum (unilateral) limited to a single component at $f = f_0$. However, it occupies a time range from $-\infty$ to $+\infty$.

We will now consider the quantitative aspects of these statements. To do this, we need to introduce the notions of temporal and frequency dispersion.

A2.3.7.1. *Temporal dispersion*

The temporal dispersion σ_t of a signal $\psi(t)$ is defined in a way similar to the standard deviation of a random signal:

$$\sigma_t = \left(\frac{\int \left(t - \bar{t}\right)^2 . \left|\psi(t)\right|^2 .dt}{\int \left|\psi(t)\right|^2 .dt} \right)^{1/2} \qquad \text{[A2.83]}$$

where $\bar{t}$ is the temporal barycenter of the signal:

$$\bar{t} = \int t.\psi(t) .dt \qquad \text{[A2.84]}$$

A2.3.7.2. *Frequency dispersion*

A similar approach is used to calculate the frequency dispersion (or, more correctly, the dispersion of the angular frequency $\omega = 2\pi f$):

$$\sigma_\omega = \left(\frac{\int (\omega - \overline{\omega})^2 . |\Psi(\omega)|^2 .d\omega}{\int |\Psi(\omega)|^2 .d\omega} \right)^{1/2} \qquad [A2.85]$$

where $\Psi(\omega = 2\pi.f) = \mathcal{F}[\psi(t)]$ with a frequency barycenter $\overline{\omega}$ defined as follows:

$$\overline{\omega} = \int \omega.\Psi(\omega) .d\omega \qquad [A2.86]$$

A2.3.7.3. *Heisenberg–Gabor inequality*

This inequality, applied to any given signal $\psi(t)$, may be summarized as:

$$\sigma_t.\sigma_\omega \geq \frac{1}{2} \qquad [A2.87]$$

REMARK A2.8.– The demonstration of this inequality lies outside the scope of this book, but further details may be found in [DEG 01].

A2.3.8. *"Time/frequency" optimal signal*

We may use inequality [A2.87] to consider the form of the signal $\psi(t)$ which allows us to reach a situation of equality, which may be considered to be optimal. It is possible to verify that this result is obtained for a Gaussian signal $g(t)$:

$$g(t) = \frac{1}{\sigma_t\sqrt{2\pi}}.e^{-\frac{t^2}{2\sigma_t^2}} \qquad [A2.88]$$

Note that this signal is centered on instant $t = 0$, and the temporal dispersion σ_t appears explicitly in the expression.

Moreover, the Fourier transform of a Gaussian signal is also Gaussian:

$$G(\omega) = e^{-\sigma_t^2 \omega^2} \qquad \text{[A2.89]}$$

Using the analogy between the two expressions [A2.88] and [A2.89], the angular frequency distribution σ_ω may be obtained without calculation:

$$\sigma_\omega = \frac{1}{2\sigma_t} \qquad \text{[A2.90]}$$

We, therefore, clearly see that the minimum boundary of the product $\sigma_t.\sigma_\omega$ is reached in this case.

A2.4. PWM and distortion analysis

In this section, we will consider the quality of the power supply to a load in permanent sinusoidal load provided by an inverter (in both single- and three-phase contexts). In this case, we will presume that the inverter and power supply are ideal:

– a strictly constant voltage source entering the inverter;

– instantaneous switch commutation;

– no deadtime in switching in half-bridges;

– zero voltage drop-off at the switch terminals in ON state.

Evidently, the voltage $v(t)$ supplied to the load has a finite number of possible values, due to the switching function of the converter used in the power supply. This value is a piecewise constant (i.e. constant for given time intervals). However, using PWM, the sliding average of this voltage needs to follow a reference sinusoid with fixed amplitude and frequency values. The load, generally of the R, L, E type for an electrical machine, behaves as a low-pass filter which eliminates (or at least significantly limits) the high-frequency

components of the current. This specific value is key in evaluating the quality of the power supply to a machine, as it is central to the torque generated by the machine in relation to the mechanical load.

Since a machine is a complex piece of equipment, the characterization of a PWM strategy in terms of distortion requires the use of mathematical tools, which must be sufficiently representative of the real load and sufficiently simple to enable effective study. Generally, an evaluation of the integral of the voltage wave is used to evaluate the distortion created by a command in comparison with both the ideal case and a number of other command techniques.

This methodology is applicable to both single- and three-phase inverters. However, in the case of a three-phase inverter, we use a vector-based approach to model the inverter, with an equivalent two-phase representation of the voltage (and current) output of the inverter. Despite this difference, we will systematically consider an inverter output voltage waveform $v(t)$, in comparison with the desired sinusoidal wave $v_{\mathrm{ref}}(t)$. The induced error, denoted as $\Delta(t) = v(t) - v_{\mathrm{ref}}(t)$, is then integrated to obtain a signal denoted as $\Sigma(t) = \int \Delta(t).dt$. We then evaluate the RMS value of this signal over a period F_m of the reference wave $v_{\mathrm{ref}}(t)$.

Clearly, a certain number of additional parameters have an effect on the result:

– the direct current (DC) bus voltage V_{dc} powering the inverter;

– the amplitude of the reference voltage $V_{\mathrm{ref}}^{\mathrm{max}}$;

– the switching frequency F_d.

In practice, these parameters may be condensed to give two normalized parameters:

– the modulation depth $K_m = 2V_{\text{ref}}^{\max}/V_{\text{dc}}$;

– the frequency ration $K_f = F_d/F_m$.

A2.4.1. *Single-phase inverters*

In a single-phase context, only two fixed-frequency command variations may be envisaged for an H-bridge, single-phase inverter. Two types of PWM may be used:

– bipolar PWM (with complementary control of the two half-bridges, giving a voltage of $v(t) \in \{-V_{\text{dc}}; +V_{\text{dc}}\}$);

– unipolar PWM (with one half-bridge in the ON state for each half-alternation of $v_{ref}(t)$, giving a voltage of $v(t) \in \{-V_{\text{dc}}; 0; +V_{\text{dc}}\}$).

In comparing the two strategies, we have chosen to use the THD of the integral of the error between $v(t)$ and $v_{ref}(t)$ (v_{ref} is sinusoidal, with a period $T_m = 1/F_m$):

$$\text{THD}_{weighted} = \frac{\sqrt{\frac{1}{T_m}\int_0^{T_m}\left(\int_0^t v(\tau) - v_{ref}(\tau)d\tau\right)^2 .dt}}{V_{\text{ref}}^{\max}/\sqrt{2}} \qquad \text{[A2.91]}$$

The logarithm of this distortion rate ($\log(\text{THD}_{pond})$) for both modulation types is presented in Figure A2.3.

We immediately see that the distortion resulting from unipolar PWM is significantly lower for a given pairing (K_f, K_m) than the distortion involved in bipolar PWM. In qualitative terms, this result can be explained by the fact that the voltage peaks induced by unipolar PWM are half the size of those induced by bipolar PWM (V_{dc} instead of $2V_{\text{dc}}$), as shown in Chapter 2 of this volume.

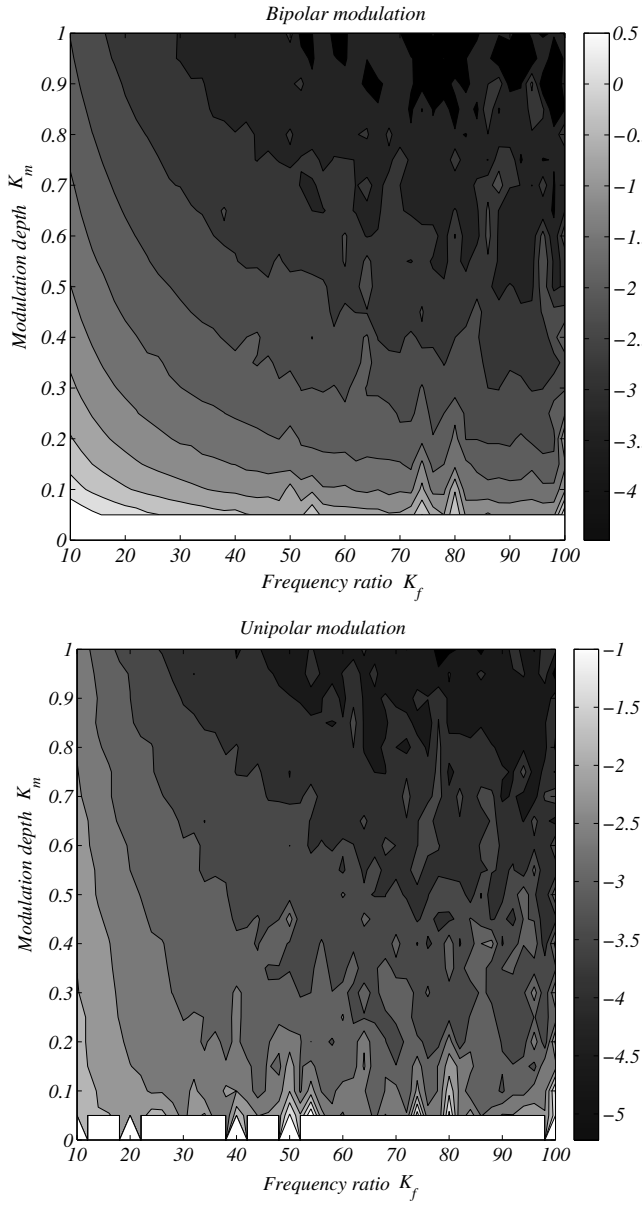


Figure A2.3. *Comparison of distortions resulting from bipolar and unipolar PWM*

A2.4.2. *Three-phase inverters*

The same analytical approach may be used for three-phase inverters, but it no longer applies to a scalar voltage $v(t)$, but rather to a two-phase voltage vector, expressed in the stationary plane (α, β)[6].

Several calculation methods have been proposed [HAV 99, NAR 08, NAR 06, ZHA 10]; here, we have chosen to use a method developed by Hava [HAV 98] due to its simplicity of implementation.

Using the hypothesis $F_d \gg F_m$, the three reference voltages are always considered to be constant at the level of the switching period $T_d = 1/F_d$. From a vector perspective in the plane (α, β), the normalized reference vector (in relation to $\frac{V_{dc}}{2}$) $\overrightarrow{V^*}$ is, therefore, considered to be constant for each switching period, and may be expressed using the equivalent phaser $\overline{V^*}$:

$$\overline{V^*} = m \times e^{j\theta} \qquad \text{[A2.92]}$$

where $\theta = \omega t$, which is the angle between the reference vector and axis α, and ω is the angular speed of rotation of the reference vector.

In this case, the SVPWM strategy may be used to illustrate this principle.

In sector I of the hexagon in the plane $\alpha\beta$, for a raising-lowering-type carrier, the following symmetrical sequence is applied for each switching period: 7-2-1-0-0-1-2-7 (where 7 represents the vector $\overrightarrow{V_7}$) (inverse configuration in relation to that used in Figure 2.15 of this volume,

6 This approach can also be applied to quantities expressed in a rotating plane (d, q): both formalisms are used in the literature on the subject, but note that the results obtained are strictly equivalent.

Chapter 2). When a normalized output vector of the inverter $\overrightarrow{V_i}$ is applied, an instantaneous error vector (or harmonic vector) is deduced using the following relationship:

$$\overrightarrow{\Delta_i} = \frac{v_{\mathrm{dc}}}{2} \times \underbrace{(\overrightarrow{V_i} - \overrightarrow{V^*})}_{\overrightarrow{\delta_i}} \qquad \text{[A2.93]}$$

where $\overrightarrow{\delta_i}$, dependent on m, θ and $\overrightarrow{V_i}$, is the normalized vector in relation to $V_{\mathrm{dc}}/2$ of vector $\overrightarrow{\Delta_i}$.

This voltage error $\overrightarrow{\Delta_i}$ is, evidently, measured in volts, and vector $\overrightarrow{\delta_i}$ has no unit.

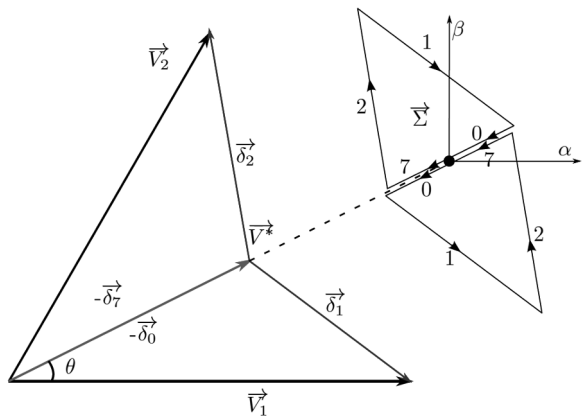


Figure A2.4. *Trajectory of the harmonic flux during a switching period for the SVPWM strategy*

Figure A2.4 shows the different error vectors corresponding to a reference vector situated in sector I of the hexagon. We see that the amplitude and phase of the error vectors are dependent on the amplitude (and thus the modulation index m) and the position of the reference vector (and thus on angle θ).

The cumulated voltage error is defined by the following formula:

$$\overrightarrow{\Sigma} = \int \overrightarrow{\Delta_i} dt = \frac{v_{dc}}{2} \times \int \overrightarrow{\delta_i}\, dt \qquad \text{[A2.94]}$$

This quantity $\overrightarrow{\Sigma}$ is the integral of a voltage, and is equivalent (following Faraday's law) to a magnetic flux. This flux is known as the conceptual harmonic flux.

Using a classic $R - L(-E)$ model of electrical machines (this time using three phases), the role of the inductive component is more important than that of the resistive component at switching period level. As the origin of the current harmonics is the error between the voltage applied at the inverter output and the reference voltage, the following relationship between the harmonics of the load currents I_h and the integral of the voltage error vector reveals the nature of the "conceptual" flux of vector Σ:

$$\overrightarrow{\Sigma} = L \times \overrightarrow{I_h} \qquad \text{[A2.95]}$$

Consequently, the study of $\overrightarrow{\Sigma}$ is equivalent to the study of $\overrightarrow{I_h}$. Note that the calculation of the conceptual harmonic flow requires no information concerning the load, and is characteristic of the chosen PWM strategy. The trajectory of $\overrightarrow{\Sigma}$ corresponding to the SVPWM strategy over a switching period is illustrated in Figure A2.4. Let us suppose that, at the start of the first switching period, $\overrightarrow{\Sigma}$ starts from 0: it returns to 0 in the middle and at the end of the switching period (this is repeated for all periods). The trajectory shown in Figure A2.4 corresponds to the 7-2-1-0-0-1-2-7 sequence, with equal application times for vectors $\overrightarrow{V_0}$ and $\overrightarrow{V_7}$. As intersective PWM strategies with raising lowering-type carriers only generate symmetrical switching sequences, it is sufficient to calculate $\overrightarrow{\Sigma}$ for half of the switching period, and the trajectory of $\overrightarrow{\Sigma}$ for the second half of the period is exactly

symmetrical to that of the first half. Furthermore, each PWM strategy involves a different distribution of the application times of free wheel vectors; consequently, the trajectory of $\overrightarrow{\Sigma}$ for each PWM strategy is unique (we do not, therefore, obtain results by PWM family, as in the case of $\overline{I_{dc}}$).

We will now present the method used to calculate the RMS value of the modulus of $\overrightarrow{\Sigma}$ over a fundamental period; symmetry in the plane $\alpha\beta$ means that only a sector of $\frac{\pi}{3}$ $(60°)$ needs to be analyzed.

First, variable changes may be used to express the harmonic flux over half a switching period as:

$$\overrightarrow{\Sigma} = \Sigma_0 \times \overrightarrow{\sigma} \qquad \text{[A2.96]}$$

where $\Sigma_0 = \frac{v_{dc}}{2}\frac{T_d}{2}$ is dependent on the DC bus voltage and the switching period, and $\overrightarrow{\sigma}$ is the normalized vector in relation to Σ_0 of vector $\overrightarrow{\Sigma}$.

For the SVPWM strategy, the analytical formulation of the trajectory of phaser $\overline{\sigma}$ (associated with vector σ) is:

$$\overline{\sigma} = \begin{cases} -m \times e^{j\theta} \times y & 0 \le y \le y_7 \\ -\frac{4}{3} \times e^{j\frac{\pi}{3}} \times y_7 + (\frac{4}{3} \times e^{j\frac{\pi}{3}} - m \times e^{j\theta}) \times y & y_7 \le y \le y_2 \\ -\frac{4}{3} \times e^{j\frac{\pi}{3}} \times y_7 + \frac{4}{3} \times (e^{j\frac{\pi}{3}} - 1) \times y_2 & \\ \quad +(\frac{4}{3} - m \times e^{j\theta}) \times y & y_2 \le y \le y_1 \\ -\frac{4}{3} \times e^{j\frac{\pi}{3}} \times y_7 + \frac{4}{3} \times (e^{j\frac{\pi}{3}} - 1) \times y_2 & \\ \quad +\frac{4}{3} \times y_1 - m \times e^{j\theta} \times y & y_1 \le y \le 1 \end{cases} \qquad \text{[A2.97]}$$

where $y_7 = \frac{t_7}{T_d}$, $y_2 = y_7 + \frac{t_2}{T_d}$, $y_1 = y_2 + \frac{t_1}{T_d}$ are coefficients imposed by projections of the reference vector onto the vectors used during the switching period (in this case, $\overrightarrow{V_1}$ and $\overrightarrow{V_2}$). Next, the switching period is filled in by applying the null vectors $\overrightarrow{V_0}$ and $\overrightarrow{V_7}$ (used for the same periods as in classic PWM).

The RMS value of vector $\overrightarrow{\sigma}$ over a fundamental period, which we will denote by ψ_f, may be calculated following the method explained in Appendix 1. The relationship between the RMS value of $\overrightarrow{\Sigma}$ over a fundamental period $RMS(\left\|\overrightarrow{\Sigma}\right\|)$ and ψ_f is as follows:

$$RMS(\left\|\overrightarrow{\Sigma}\right\|) = \Sigma_0 \times \psi_f \qquad \text{[A2.98]}$$

In other words, ψ_f is the normalized value in relation to Σ_0 of the RMS value of $\overrightarrow{\Sigma}$ over a fundamental period. In the following, ψ_f will be used as a tool for comparing strategies.

Using the same PWM strategy, by increasing the switching frequency, we reduce the value of T_d, and consequently the value of Σ_0. In qualitative terms, this relates to the fact that current harmonics are reduced as the switching frequency increases. In order to compare different PWM strategies, the same switching frequency must be used in all cases; this comes down to comparing strategies using the value of ψ_f, which is independent of the switching frequency. Clearly, from this perspective, the best strategies will present the lowest value for ψ_f (reduced ripple in load currents).

The value of ψ_f for the SVPWM strategy may be obtained using the following formula [HAV 98]:

$$\psi_f(m) = \sqrt{\frac{3}{\pi}\left[\frac{\pi}{36}m^2 - \frac{2\sqrt{3}}{27}m^3 + \left(\frac{\pi}{32} - \frac{3\sqrt{3}}{128}\right)m^4\right]} \qquad \text{[A2.99]}$$

This analytical expression is particularly interesting as the SVPWM strategy is generally considered in published literature as a benchmark for the evaluation of other techniques.

Figure A2.5 shows its appearance as a function of m. This curve is applicable for all values φ of the phase deviation between currents and voltages in a load.

A2.5. Spectral analysis of the DC bus current

The method presented in section A2.2.3 allows us not only to calculate the spectrum of inverter output voltages but also the spectrum of the inverter input current. Bierhoff *et al.* [BIE 08] applied the method proposed by Black [BLA 53] for different PWM strategies, based on the double Fourier series decomposition. We will not go into detail concerning this work here, but useful information on this subject may also be found in [NGU 11a].

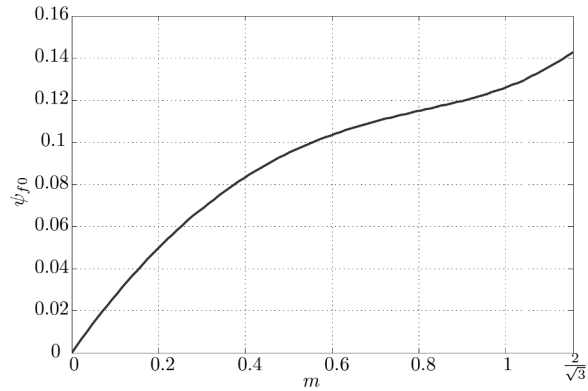


Figure A2.5. *RMS value of the normalized harmonic flow for the SVPWM strategy as a function of* m *in the linear zone*

Bibliography

[ALE 05] ALEXANDER M., Power Distribution System (PDS) Design: Using Bypass/Decoupling Capacitors, Application Note, XAPP623, February 2005. Available from www.xilinx.com.

[APP 02] APPEL W., *Mathématiques pour la physique et les physiciens*, H & K, Paris, 2002.

[BAS 09] BASDEVANT J.-L., *Les mathématiques de la physique quantique*, Vuibert, Paris, 2009.

[BEC 00] BECH M.M., Analysis of random pulse-width modulation techniques for power electronic converters, PhD Thesis, Aalborg University, 2000.

[BEN 33] BENNETT W.R., "New results in the calculation of modulation productions", *Bell Systems Technical Journal*, vol. 12, no. 4, pp. 238–243, 1933.

[BIE 08] BIERHOFF M., FUCHS F.W., "DC link harmonics of three phase voltage source converters influenced by the pulsewidth modulation strategy – an analysis", *IEEE Transactions on Industrial Electronics*, vol. 55, no. 5, pp. 2085–2092, May 2008.

[BLA 53] BLACK H.S., *Modulation Theories*, Van Nostrand, New York, NY, 1953.

[BOW 08] BOWICK C., BLYLER J., AJLUNI C., *RF Circuit Design*, Newnes/Elsevier, Boston, Amsterdam, 2008.

[BRÉ 05] BRÉHAUT S., Modélisation et optimisation des performances CEM d'un convertisseur AC/DC d'une puissance de 600 W, Doctoral Thesis, François Rabelais University, Tours, 2005.

[BÜH 91] BÜHLER H., *Convertisseurs Statiques*, Presses polytechniques et universitaires Romandes, Lausanne, 1991.

[CHA 05] CHAROY A., *Compatibilité Électromagnétique*, Dunod, Paris, 2005.

[CHE 09] CHENAND L., PENG F.Z., "Closed-loop gate drive for high power IGBTs", *Proceedings of the IEEE APEC*, pp. 1331–1337, 2009.

[CHE 99] CHERON Y., *La Commutation Douce*, Tec & Doc, Paris, 1999.

[COH 00] COHEN DE LARA M., D'ANDRÉA-NOVEL B., *Cours d'Automatique – Commande Linéaire des Systèmes Dynamiques*, Mines Press, Paris, 2000.

[COC 02] COCQUERELLE J.-L., PASQUIER C., *Rayonnement Électromagnétique des Convertisseurs à découpage*, EDP Sciences, Les Ulis, 2002.

[COR 13] CORNELL D., Aluminum electrolytic capacitor application guide, available at www.cde.com/fliptest/ alum/alum.html, 2013.

[COS 05] COSTA F., MAGNON D., "Graphical analysis of the spectra of EMI sources in power electronics", *IEEE Transactions on Power Electronics*, vol. 20, no. 6, pp. 1491–1498, November 2005.

[COS 13] COSTA F., GAUTIER C., LABOURÉ E., *et al.*, *La compatibilité électromagnétique en électronique de puissance*, *Principes et cas d'études*, Hermes-Lavoisier, Paris, 2013.

[DEG 01] DEGRANGE B., *Introduction à La Physique Quantique*, Mines Press, Paris, 2001.

[DEL 01] DELABALLE J., La CEM: la compatibilité électromagnétique, *Technical Specifications, Schneider Electric*, vol. 149, 2001.

[FER 02] FERRIEUX J.-P., FOREST F., *Alimentations à découpages et Convertisseurs à Résonance*, 3rd ed., Dunod, Paris, 2002.

[FEY 99] FEYNMAN R., LEIGHTON R.B., SANDS M., *Cours de Physique de Feynman, Electromagnétisme*, Dunod, vols. 1–2, Paris, 1999.

[FOC 98] FOCH H., FOREST F., MEYNARD T., "Onduleurs de tension – structures, principes, applications", *Techniques de L'Ingénieur*, Article D3176, Traité Génie Electrique, 1998.

[FOC 94] FOCH H., CHÉRON Y., "Convertisseur de type forward – dimensionnement", *Techniques de L'ingénieur*, Article D3167, Traité Génie Electrique, 1994.

[FRI 94] FRICKEY D.A., "Conversions between S, Z, Y, h, ABCD, and T parameters which are valid for complex source and load impedances", *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, no. 2, pp. 205–211, 1994.

[GHA 03] GHAUSI M., LAKER K., *Modern Filter Design: Active RC and Switched Capacitor*, Noble Publishing, Atlanta, 2003.

[GIB 07] GIBSON W.C., *The Method of Moments in Electromagnetics*, Chapman & Hall/CRC, Boca Raton, FL, 2007.

[HAV 98] HAVA A.M., KERKMAN R.J., LIPO T.A., "A high performance generalized discontinuous PWM algorithm", *IEEE Transactions on Industry Applications*, vol. 34, no. 5, pp. 1059–1071, 1998.

[HAV 99] HAVA A.M., LIPO T.A., KERKMAN R.J., "Simple analytical and graphical methods for carrier-based PWM-VSI drives", *IEEE Transactions on Power Electronics*, vol. 14, no. 1, pp. 49–61, 1999.

[HOB 05] HOBRAICHE J., Comparaison des stratégies de modulation à largeur d'impulsions triphasées – application à l'alterno-démarreur, Doctoral Thesis, UTC, Compiègne, 2005.

[HOL 83] HOLTZ J., STADTFELD S., "A predictive controller for a stator current vector of AC-machines fed from a switched voltage source", *Proceedings of the International Power Electronics Conference (IPEC)*, Tokyo, vol. 2, pp. 1665–1675, 1983.

[IEE 12] IEEE Standards Association, IEEE Electromagnetic Compatibility Standards Collection: VuSpec^{TM}, CD-ROM, 2012.

[KEM 14] KEMET, Electrolytic Capacitors, technical document, FF3304, available at www.kemet.com/lists/ProductCatolog/attachments/235/F3304.pdf, 2014.

[KOL 91] KOLAR J.W., ERLT H., ZACH F.C., "Influence of the modulation method on the conduction and switching losses of a PWM converter system", *IEEE Transactions on Industry Applications*, vol. 27, no. 6, pp. 399–403, 1991.

[KOL 93] KOLAR J.W., Vorrichtung und Verfahren zur Umformung von Drehstrom in Gleichstrom, IXYS Semiconductors GmdH, Patent no. EP0660498 A: 23 December 1993.

[LAN 09] LANFRANCHI V., PATIN N., DÉPERNET D., "MLI précalculées et optimisées", in MONMASSON E., (ed.), *Commande Rapprochée de Convertisseurs*, Hermes-Lavoisier, Paris, 2009.

[LEF 02] LEFEBVRE S., MULTON B., "Commande des semi-conducteurs de puissance: principes", *Techniques de l'Ingénieur*, D-3231, 2002.

[LES 97] LESBROUSSARD C., Etude d'une stratégie de modulation de largeur d'impulsions pour un onduleur de tension triphasé à deux ou trois niveaux: la Modulation Delta Sigma Vectorielle, Doctoral Thesis, UTC, 1997.

[LIN 10] LINDER A., KANCHAN R., KENNEL R., *et al.*, *Model-Based Predictive Control of Electrical Drives*, Cuvillier Verlag, Gttingen, 2010.

[LUM 00] LUMBROSO H., *Ondes Électromagnétiques Dans le Vide et les Conducteurs, 70 Problèmes Résolus*, 2nd ed., Dunod, Paris, 2000.

[MAT 09] MATHIEU H., FANET H., *Physique des Semiconducteurs et des Composants*, 6th ed., Dunod, Paris, 2009.

[MEY 93] MEYNARD T., FOCH H., "Imbricated cells multilevel voltage-source inverters for high-voltage applications", *EPE Journal*, vol. 3, no. 2, pp. 99–101, June 1993.

[MIC 05] MICROCHIP, Sinusoidal control of PMSM motors with dsPIC30F3010, AN1017, available at ww1.microchip.com/downloads/en/AppNotes/01017A.pdf, 2005.

[MID 77] MIDDLEBROOK R.D., CK S., "A general unified approach to modeling switching converter power stages", *International Journal of Electronics*, vol. 42, no. 6, pp. 521–550, 1977.

[MOH 95] MOHAN N., UNDELAND T.M., ROBBINS W.P., *Power Electronics – Converters, Applications and Design*, 2nd ed., Wiley, New York, NY, 1995.

[MON 97] MONMASSON E., FAUCHER J., "Projet pédagogique autour de la MLI vectorielle", *Revue,* vol. 3EI, no. 8, pp. 22–36, 1997.

[MON 09] MONMASSON E., (ed.), *Controle Rapprochée de Convertisseurs Statiques 1, Modulation de Largeur d'Impulsion*, Hermes-Lavoisier, Paris, 2009.

[MON 11] MONMASSON E., (ed.), *Power Electronic Converters: PWM Strategies and Current Control Techniques*, ISTE, London and John Wiley & Sons, New York, 2011.

[MOR 07] MOREL F., Commandes directes appliquées à une machine synchrone à aimants permanents alimentée par un onduleur triphasé à deux niveaux ou par un convertisseur matriciel triphasé, Doctoral Thesis, INSA, Lyon, 2007.

[MOY 98] MOYNIHAN J.F., EGAN M.G., MURPHY J.M.D., "Theoretical spectra of space vector modulated waveforms", *IEE Proceedings Electrical Power Applications*, vol. 145, pp. 17–24, 1998.

[MUK 10] MUKHTAR A., *High Performance AC Drives*, Springer, Berlin, 2010.

[NAR 06] NARAYANAN G., KRISHNAMURTHY H.K., ZHAO D., *et al.*, "Advanced bus-clamping PWM techniques based on space vector approach", *IEEE Transactions on Power Electronics*, vol. 21, no. 4, pp. 974–984, 2006.

[NAR 08] NARAYANAN G., RANGANATHAN V.T., ZHAO D., *et al.*, "Space vector based hybrid PWM techniques for reduced current ripple", *IEEE Transactions on Industrial Electronics*, vol. 55, no. 4, pp. 1614–1627, 2008.

[NGU 11a] NGUYEN T.D., Etude de stratégies de modulation pour onduleur triphasé dédiées à la réduction des perturbations du bus continu en environnement embarqué, Doctoral Thesis, UTC, Compiègne, 2011.

[NGU 11b] NGUYEN T.D., HOBRAICHE J., PATIN N., *et al.*, "A direct digital technique implementation of general discontinuous pulse width modulation strategy", *IEEE Transactions on Industrial Electronics*, vol. 58, no. 9, pp. 4445–4454, September 2011.

[OSW 11] OSWALD N., STARK B., HOLLIDAY D., *et al.*, "Analysis of shaped pulse transitions in power electronic switching waveforms for reduced EMI generation", *IEEE Transactions on Industry Applications*, vol. 47, no. 5, pp. 2154–2165, October–November 2011.

[PAT 15a] PATIN N., *Power Electronics Applied to Industrial Systems and Transport – Volume 1*, ISTE Press Ltd., London and Elsevier Ltd., Oxford, 2015.

[PAT 15b] PATIN N., *Power Electronics Applied to Industrial Systems and Transport – Volume 3*, ISTE Press Ltd., London and Elsevier Ltd., Oxford, 2015.

[PAT 15c] PATIN N., *Power Electronics Applied to Industrial Systems and Transport – Volume 4*, ISTE Press Ltd., London and Elsevier Ltd., Oxford, 2015.

[REB 98] REBY F., BAUSIERE R., SOHIER B., *et al.*, "Reduction of radiated and conducted emissions in power electronic circuits by the continuous derivative control method (CDCM)", *Proceedings of the 7th International Conference on Power Electron, Variable Speed Drives*, pp. 158–162, 1998.

[REV 03] REVOL B., Modélisation et optimisation des performances CEM d'une association variateur de vitesse machine asynchrone, Doctoral Thesis, Joseph Fourier University, 2003.

[ROM 86] ROMBAULT C., SÉGUIER G., BAUSIÈRE R., *L'électronique de puissance – Volume 2, La conversion AC-AC*, Tec & Doc, Paris, 1986.

[ROU 04a] ROUDET J., CLAVEL E., GUICHON J.M., *et al.*, "Modélisation PEEC des connexions dans les convertisseurs de puissance", *Techniques de l'Ingénieur*, D-3071, 2004.

[ROU 04b] ROUDET J., CLAVEL E., GUICHON J.M., SCHANEN J.L., "Application de la méthode PEEC au cablage d'un onduleur triphasé", *Techniques de l'Ingénieur*, D-3072, 2004.

[ROU 04c] ROUSSEL J.-M., *Problèmes d'Électronique de Puissance*, Dunod, Paris, 2004.

[SCH 99] SCHELLMANNS A., Circuits équivalents pour transformateurs multienroulements, Application à la CEM conduite d'un convertisseur, Doctoral Thesis, l'INPG, July 1999.

[SEG 11] SÉGUIER G., DELARUE P., LABRIQUE F., *Electronique de puissance*, Dunod, Paris, 2011.

[SHU 11] SHUKLA A., GHOSH A., JOSHI A., "Natural balancing of flying capacitor voltages in multicell inverter under PD carrier-based PWM", *IEEE Transactions on Power Electronics*, vol. 56, no. 6, pp. 1682–1693, June 2011.

[VAS 12] VASCAS F., IANNELI L., (eds), *Dynamics and Control of Switched Electronic Systems*, Springer, Berlin, 2012.

[VEN 07] VENET P., Amélioration de la sûreté de fonctionnement des dispositifs de stockage d'énergie, mémoire d'HDR, Claude Bernard University – Lyon 1, 2007

[VIS 07] VISSER J.H., Active converter based on the vienna rectifier topology interfacing a three-phase generator to a DC-Bus, Master's Thesis, University of Pretoria, South Africa, 2007.

[VIS 12] VISSER H.J., *Antenna Theory and Applications*, Wiley, New York, NY, 2012.

[VOG 11] VOGELSBERGER M.A., WIESINGER T., ERTL H., "Life-cycle monitoring and voltage-managing unit for DC-link electrolytic capacitors in PWM converters", *IEEE Transactions on Power Electronics*, vol. 26, no. 2, pp. 493–503, February 2011.

[WEE 06] WEENS Y., Modélisation des cables d'énergie soumis aux contraintes générées par les convertisseurs électroniques de puissance, Doctoral Thesis, USTL, Lille, 2006.

[WHE 04] WHEELER P.W., CLARE J.C., EMPRINGHAM L., *et al.*, "Matrix converters", *IEEE Industry Applications Magazine*, vol. 10, no. 1, pp. 59–65, January–February 2004.

[WIL 99] WILLIAMS T., *Compatibilité électromagnétique – De la Conception à l'Homologation*, Publitronic, Paris, 1999.

[YUA 00] YUAN X., BARBI I., "Fundamentals of a new diode clamping multilevel inverter", *IEEE Transactions on Power Electronics*, vol. 15, no. 4, pp. 711–718, July 2000.

[ZHA 10] ZHAO D., HARI V.S.S.P.K., NARAYANAN G., *et al.*, "Space-vector-based hybrid pulsewidth modulation techniques for reduced harmonic distortion and switching loss", *IEEE Transactions on Power Electronics*, vol. 25, no. 3, pp. 760–774, 2010.

Index